

AKAI



SERVICE MANUAL

Model: LCT37Z6TA

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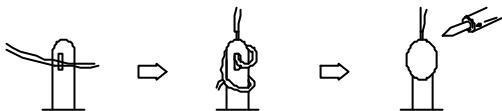
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: This manual is the latest at the time of printing, and does not
: include the modification which may be made after the printing,
: by the constant improvement of product.
:

I. Safety Instructions

 <div style="border: 1px solid black; padding: 5px; text-align: center;">CAUTION RISK OF ELECTRIC SHOCK DO NOT OPEN</div> 	<p>The lightning flash with arrowhead symbol, within an equilateral triangle, is intended to alert the user to the presence of uninsulated "dangerous voltage" within the product's enclosure that may be of sufficient magnitude to constitute a risk of electric shock to persons.</p> <p>The exclamation point within an equilateral triangle is intended to alert the user to the presence of important operating and maintenance (servicing) instructions in the literature accompanying the appliance.</p>
<p>CAUTION: TO REDUCE THE RISK OF ELECTRIC SHOCK, DO NOT REMOVE COVER (OR BACK). NO USER-SERVICEABLE PARTS INSIDE. REFER SERVICING TO QUALIFIED SERVICE PERSONNEL ONLY.</p>	

PRECAUTIONS DURING SERVICING

1. In addition to safety, other parts and assemblies are specified for conformance with such regulations as those applying to spurious radiation. These must also be replaced only with specified replacements.
Examples: RF converters, tuner units, antenna selection switches, RF cables, noise-blocking capacitors, noise-blocking filters, etc.
2. Use specified internal Wiring. Note especially:
 - 1) Wires covered with PVC tubing
 - 2) Double insulated wires
 - 3) High voltage leads
3. Use specified insulating materials for hazardous live parts. Note especially:
 - 1) Insulating Tape
 - 2) PVC tubing
 - 3) Spacers (insulating barriers)
 - 4) Insulating sheets for transistors
 - 5) Plastic screws for fixing micro switches
4. When replacing AC primary side components (transformers, power cords, noise blocking capacitors, etc.), wrap ends of wires securely about the terminals before soldering.



5. Make sure that wires do not contact heat generating parts (heat sinks, oxide metal film resistors, fusible resistors, etc.)
6. Check if replaced wires do not contact sharply edged or pointed parts.
7. Make sure that foreign objects (screws, solder droplets, etc.) do not remain inside the set.

MAKE YOUR CONTRIBUTION TO PROTECT THE ENVIRONMENT

Used batteries with the ISO symbol for recycling as well as small accumulators (rechargeable batteries), mini-batteries (cells) and starter batteries should not be thrown into the garbage can.
Please leave them at an appropriate depot.



SAFETY INSTRUCTION

The service should not be attempted by anyone unfamiliar with the necessary instructions on this TV receiver. The following are the necessary instructions to be observed before servicing.

1. An isolation transformer should be connected in the power line between the receiver and the AC line when a service is performed on the primary of the converter transformer of the set.
2. Comply with all caution and safety related provided on the back of the cabinet, inside the cabinet, on the chassis or picture tube.
3. To avoid a shock hazard, always discharge the picture tube's anode to the chassis ground before removing the anode cap.

4. Completely discharge the high potential voltage of the picture tube before handling. The picture tube is a vacuum and if broken, the glass will explode.
5. When replacing a MAIN PCB in the cabinet, always be certain that all protective are installed properly such as control knobs, adjustment covers or shields, barriers, isolation resistor networks etc.
6. When servicing is required, observe the original lead dressing. Extra precaution should be given to assure correct lead dressing in the high voltage area.
7. Keep wires away from high voltage or high temperature components.
8. Before returning the set to the customer, always perform an AC leakage current check on the exposed metallic parts of the cabinet, such as antennas, terminals, screwheads, metal overlay, control shafts, etc., to be sure the set is safe to operate without danger of electrical shock. Plug the AC line cord directly to the AC outlet (do not use a line isolation transformer during this check). Use an AC voltmeter having 5K ohms volt sensitivity or more in the following manner.

Connect a 1.5K ohm 10 watt resistor paralleled by a 0.15 μ F AC type capacitor, between a good earth ground (water pipe, conductor etc..) and the exposed metallic parts, one at a time.

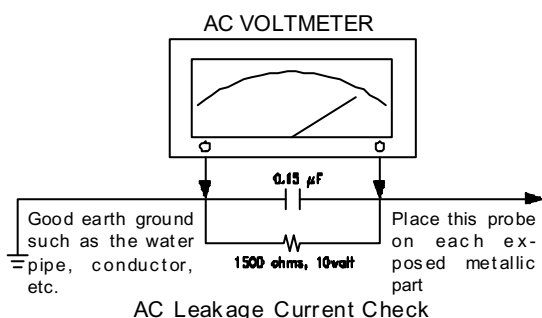
Measure the AC voltage across the combination of the 1.5K ohm resistor and 0.15 uF capacitor. Reverse the AC plug at the AC outlet and repeat the AC voltage measurements for each exposed metallic part.

The measured voltage must not exceed 0.3V RMS. This corresponds to 0.5mA AC. Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately.

The resistance measurement should be done between accessible exposed metal parts and power cord plug prongs with the power switch "ON". The resistance should be more than 6M ohms.

PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in this TV receiver have special safety-related characteristics. These characteristics are offer passed unnoticed by visual spection and the protection afforded by them cannot necessarily be obtained by using replacement components rates for a higher voltage, wattage, etc. The replacement parts which have these special safety characteristics are identified by \triangle marks on the schematic diagram and on the parts list. Before replacing any of these components, read the parts list in this manual carefully. The use of substitute replacement parts which do not have the same safety characteristics as specified in the parts list may create shock, fire, X-RAY RADIATION or other hazards.



1.Do not power on .

1.1 Please check AC cable if connect to AC plug.

Is true the connector don't connect to AC plug. Please connect it.

2.2 Please check AC cable if connect to AC power.

Is true the AC cable don't connect to AC power. Please connect it.

3.3 Please check power board of fuse if broken.

If the F1 fuse is broken, Please pull out the AC cable from AC power. Please check AC L power and AC N ground by multimeter, The read number is infinite, the fuse is broke. then look up power board if not burn out place. Is true it. Please change power board or be changed power board.

2. The power on switch of green extinguish.

2.1 The power of led(indicator light) is red light, To touch power on key when indicator light wink.

Is true that the power DC output have somewhere short circuit.

Please check connector J6, J23 .If not connector direction is wrong.

Or the mainboard somewhere of power short circuit.

3.The power is normal work ,but don't backlight.

3.1 The indicator light work normal (green light).

Please check Main board of transistor Q18 collect if not has +5v voltage.

Is true Q18 collect hasn't +5v ,To check Q18 if fail. Or to check Q18 of base if not low.

(Low is working, high don't work).

Please refer to attached sheet A circuit diagram.

3.2 Please check backlight of connector if not it direction is wrong or the connector of wire compositor direction is wrong.

3.3 To check connector panel of voltage is +24v. It's true .Then to check of the first pin if it have +5V voltage, It's true , than to check power board of +24v voltage ,It's true. The panel of backlight board is fail. The change panel of backlight board.

Please refer to attached sheet B Panel of datasheet.

4.The screen don't have picture But have backlight.

4.1 To check to panel of voltage ,To check main board of bead L69 and L57 connect if not OK.Then check the L69 and L57 of voltage is +12v(27 inch panel voltage is +5v, To check L68 and L56) . Next to check fuse F1 and connector J10 if not is +12v(27 inch panel voltage is +5v). If isn't please check power board of connector CON5 if has +12v(27 inch panel voltage is +5v).

4.2To check to main board +12 V voltage. To check to main board IC U35 of the first pin if

+5v voltage ,It's fail. It's low (close 0 v) working.

The circuit diagram follow down:

Please refer to attached sheet A circuit diagram.

5.The remote control don't be control.

6.1 The check batteries of remote control if it run out of .

6.2 To check main board of connector J21 of wire connect fastness and the connector of wire open.

Please refer to attached sheet A circuit diagram.

6.The sound don't output.

7.1 To check main board +24v voltage of connector J39, It's true not +24v voltage. Then to check power main +24v fail .

Please refer to attached sheet A circuit diagram.

7.The DTV don't detect .

7.1 To check mainboard of connector J24 and DTV mainboard of connector HA1 of FCC wire if no connect fastness.

Please refer to attached sheet C of DTV circuit diagram.

Technical Specification

Product Model	LCT37Z6TA
TV System	NTSC M, ATSC
VIDEO System	NTSC
Screen Size	37" diagonal
Display Area	820.8mm (W) x 461.7mm (H)
Aspect Ratio	16:9
External Size (with stand)	954.5mm (W) x 724.2mm (H) x 267.5mm (D)
Net Weight (with stand)	24 kg
Display Resolution	1920(H) x 1080(V) Pixels (Each pixel has R/G/B 3 color cells)
Pixel Dot Pitch	0.4275 (H) x 0.4275 (V) mm
Color	16.7 millions of colors (R/G/B each 256 scales)
Gray Scale	256 (R/G/B each 8-bit)
Brightness (Peak Value)	500cd/m ²
Contrast (Dark Room)	800:1
Sound Effect	Acoustic Cinema Enhancement
Power Supply	AC 120V, 60 Hz
Power Consumption	230W
Input Terminal	Antenna Input (F Type) x 2 (NTSC & ATSC)
	RS-232 (D-SUB 9 Pin Type) x 1 (only for ATSC)
	HDMI (Ver. 1.1) connector x 1
	VGA (D-Sub 15 Pin Type) x 1
	Component Video - YPbPr x 2 RCA Terminals
	Video Input RCA Terminals x 1
	S-Video Input Mini Din 4 Pin Terminal x 1
	Stereo, Audio x 5
Output Terminal	1 set of Audio Output Terminals (RCA, L&R)
	SPDIF (Optical) x 1 (only for ATSC)

Note: The specifications shown above may be changed without notice for quality improvement.

Support the Signal Mode

A. VGA Mode

Resolution	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
640 x 480	31.50	60.00
	37.86	72.81
800 x 600	35.16	56.25
	37.90	60.32
	46.90	75.00
	48.08	72.19
1024 x 768	48.40	60.00

B. YPbPr Mode

Resolution	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
480i	15.734	59.94
480p(720x480)	31.468	59.94
720p(1280x720)	45.00	60.00
1080i(1920x1080)	33.75	60.00
1080P(1920x1080)	67.50	60.00

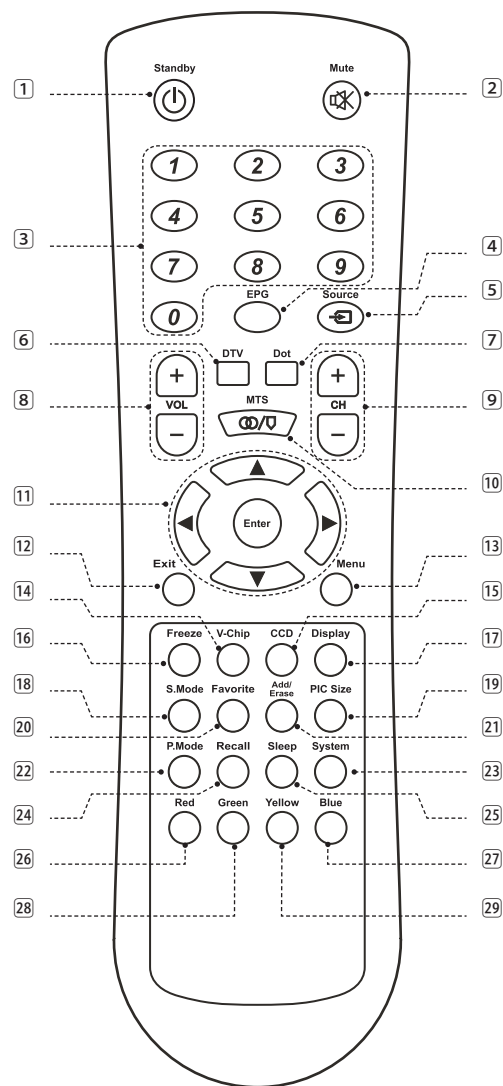
C. HDMI Mode

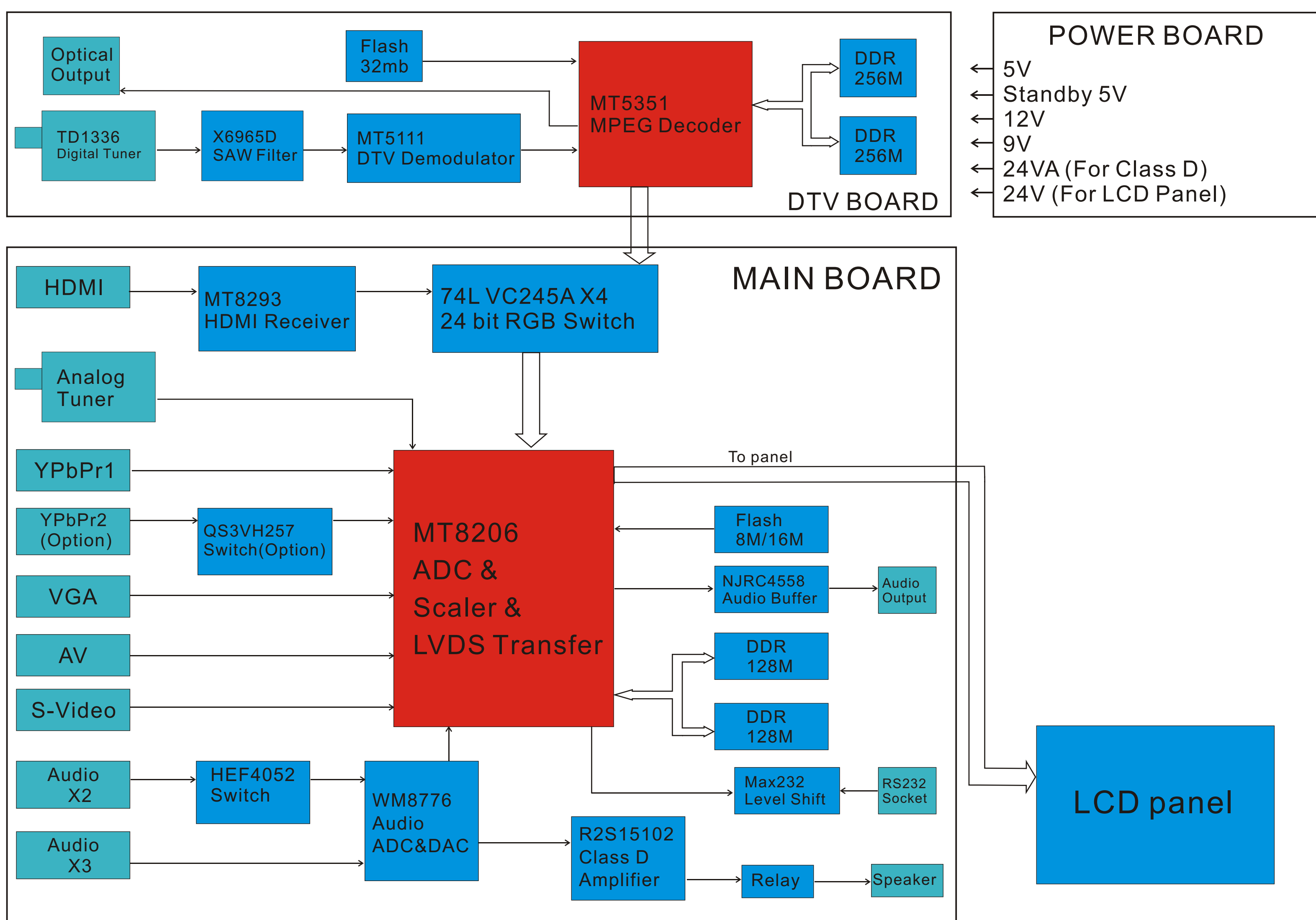
Resolution	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
480p	31.468	59.94
720p	45.00	60.00
1080i	33.75	60.00
1080P(1920x1080)	67.50	60.00

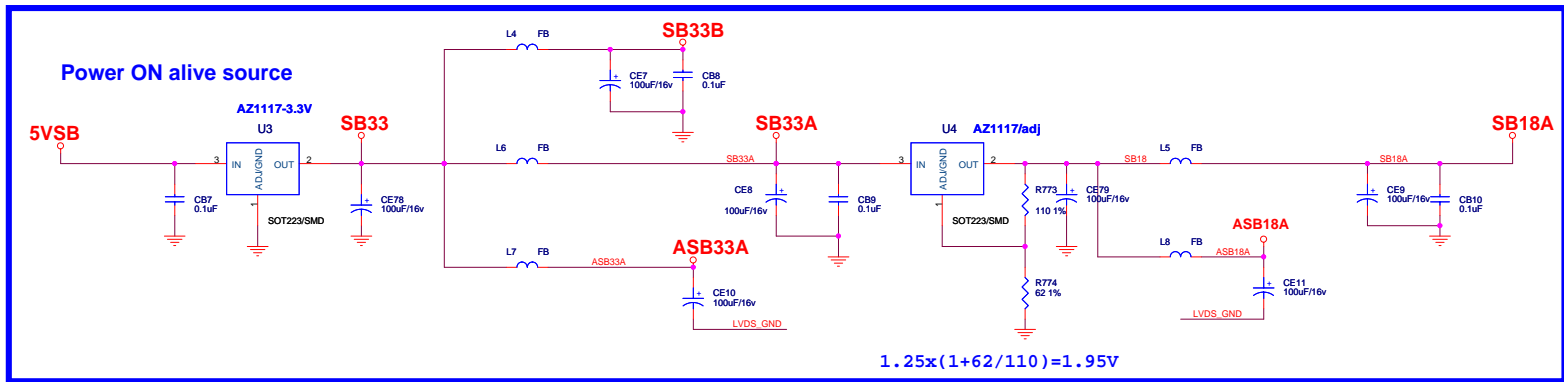
- When the signal received by the Display exceeds the allowed range, a warning message shall appear on the screen.
- You can confirm the input signal format from the on-screen.

Remote Control

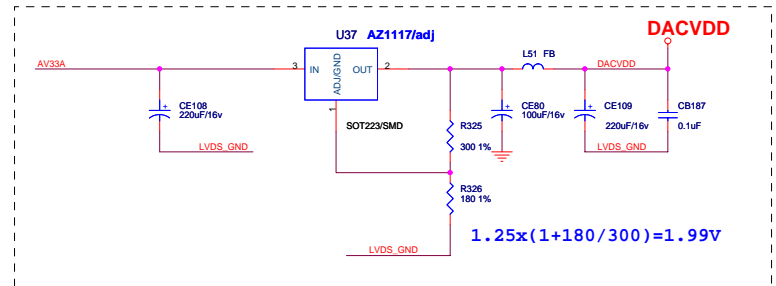
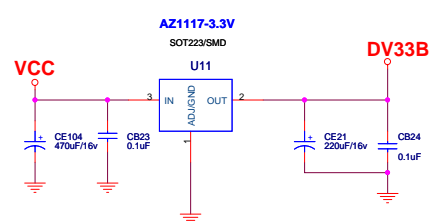
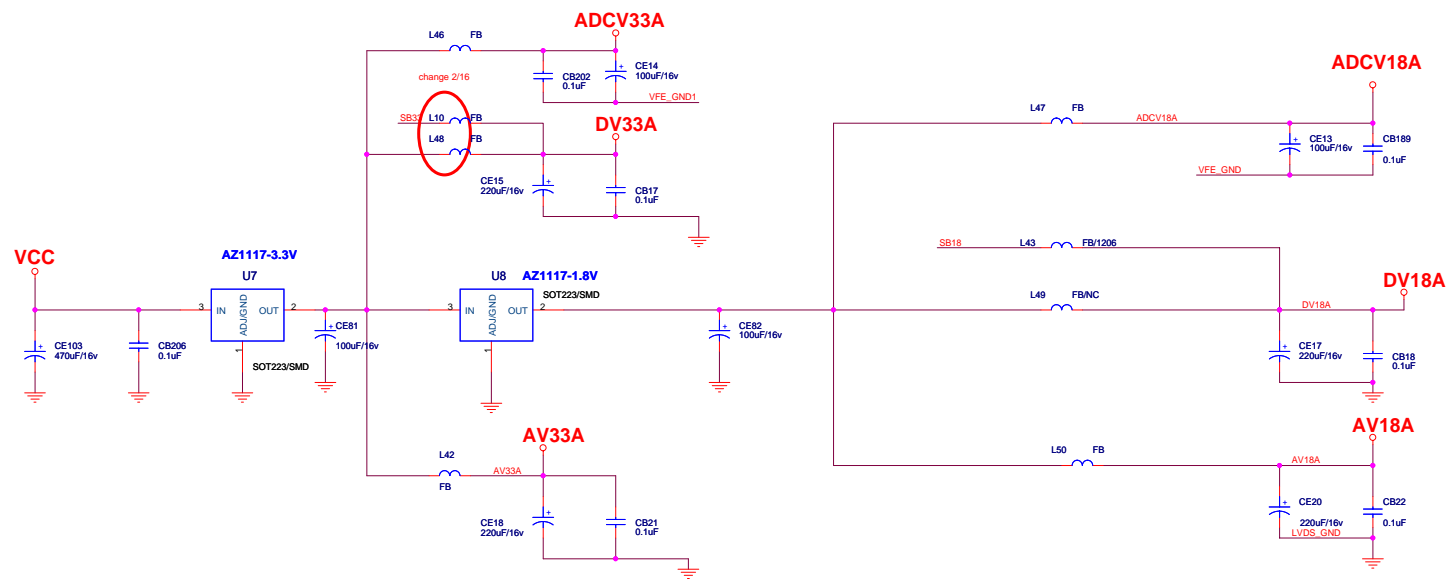
- 1 **Standby**(⏻): Press this button to turn off to standby and turn on from standby.
- 2 **Mute**(🔇): Press this button to quiet the sound system. Press again to reactivate the sound system.
- 3 **0~9 Number Buttons**: Press 0~9 to select a channel, and used to input the password; the channel changes after 2 seconds.
- 4 **EPG (Electronic Program Guide)**: Press to display EPG mode. Press again to exit EPG mode.
- 5 **Source**: Press to select the signal source, such as DTV, TV, AV, S-Video, YPbPr 1, YPbPr 2, VGA or HDMI.
- 6 **DTV**: Press to choose DTV directly.
- 7 **Dot**: Press number buttons with it to select the channels directly in DTV.
- 8 **VOL +/-**: Press to adjust the volume.
- 9 **CH +/-**: Press to select the channel forward or backward.
- 10 **MTS**: Press repeatedly to cycle through the Multi-channel TV sound (MTS) options: Mono, Stereo and SAP (Second Audio Program).
- 11 **◀, ▶, ▲, ▼, Enter**: Press **◀, ▶, ▲, ▼** to move the on-screen cursor. To select an item, press **Enter** to confirm.
- 12 **Exit**: Press this button to exit.
- 13 **Menu**: Press to enter into the on-screen setup menu, press again to exit.
- 14 **V-Chip**: Press to select the child protect mode.
- 15 **CCD**: Press to select the Closed Caption mode.
- 16 **Freeze**: Press to freeze the picture, press again to restore the picture.
(inactive for 1080i (1920x1080) in YPbPr).
- 17 **Display**: Press to display the channel information and it disappear after 3 seconds.
- 18 **S. Mode**: Press repeatedly to select the sound mode: Normal, News, Cinema, Concert and User.
- 19 **PIC Size**: Press repeatedly to cycle through the picture size. when in DTV, YPbPr1, YPbPr2 mode, it can select picture size is: Full, 4:3. While in other mode, it can select picture size is: Full, 4:3, Panoramic.
(Note: when in VGA mode, it can only select "Full".)
- 20 **Favorite**: Press repeatedly to cycle through the favorite channel list.
- 21 **Add/Erase**: Press to add or delete favorite or dislike channels.
- 22 **P. Mode**: Press repeatedly to cycle through the picture mode: Cinema, Normal, Vivid, Hi-Bright and User.
- 23 **System**: Press repeatedly to cycle through the system options: AUTO, NTSC 3.58 and PAL. (Only for AV or S-Video)
- 24 **Recall**: Press to return to previous channel.
- 25 **Sleep**: Press repeatedly until it displays the time in minutes (15 Min, 30 Min, 60 Min, 90 Min, 120 Min and, Off) that you want the TV to remain on before shutting off. To cancel sleep time, press Sleep button repeatedly until sleep Off appears.
- 26 **Red**: Press this button to access the red item or page.
- 27 **Blue**: Press this button to access the blue item or page.
- 28 **Green**: Press this button to access the green item or page.
- 29 **Yellow**: Press this button to access the yellow item or page.







- LVDS_GND >>> LVDS_GND 3.4,12
- VFE_GND >>> VFE_GND 3.4,8,11
- VFE_GND1 >>> VFE_GND1 3.4,8,11

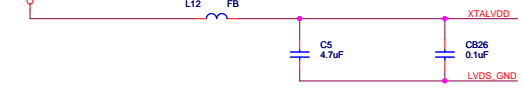


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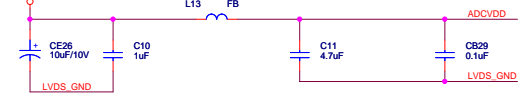
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STANDBY ANALOG POWER

ASB18A

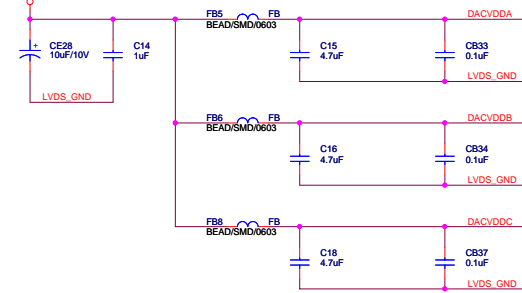


ASB33A



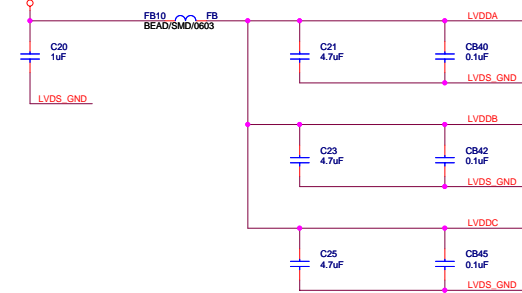
NORMAL VIDEO DAC POWER

DACVDD



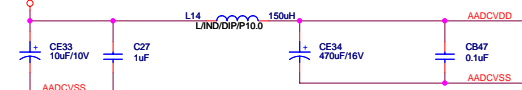
NORMAL VIDEO DAC POWER

AV33A

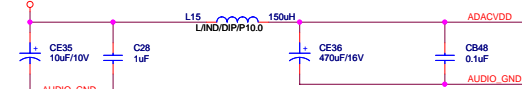


NORMAL AUDIO ADC / DAC POWER

ADCV33A

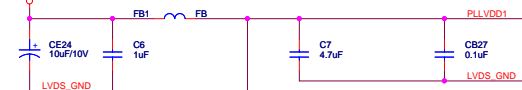


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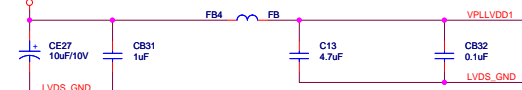


NORMAL ANALOG POWER

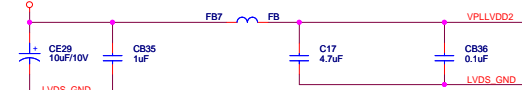
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AV18A

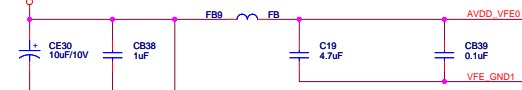


AV33A

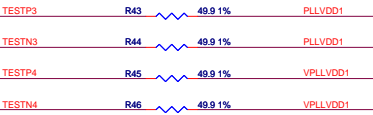
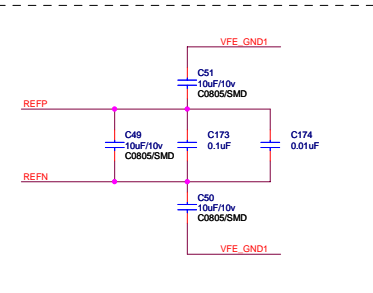
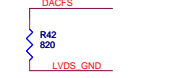
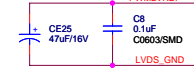
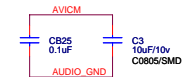
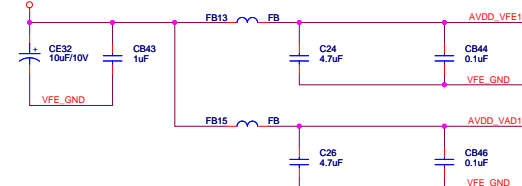


NORMAL VIDEO ADC POWER

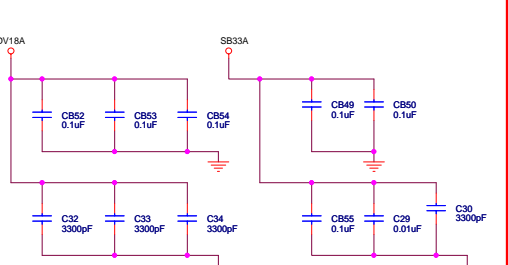
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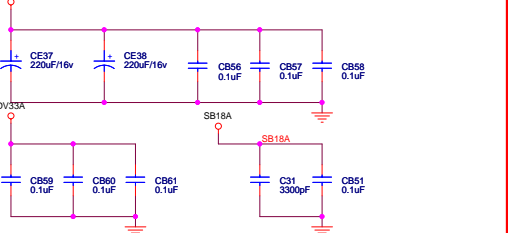
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MT8202 DIGITAL POWER & DECOUPLING



5V5B



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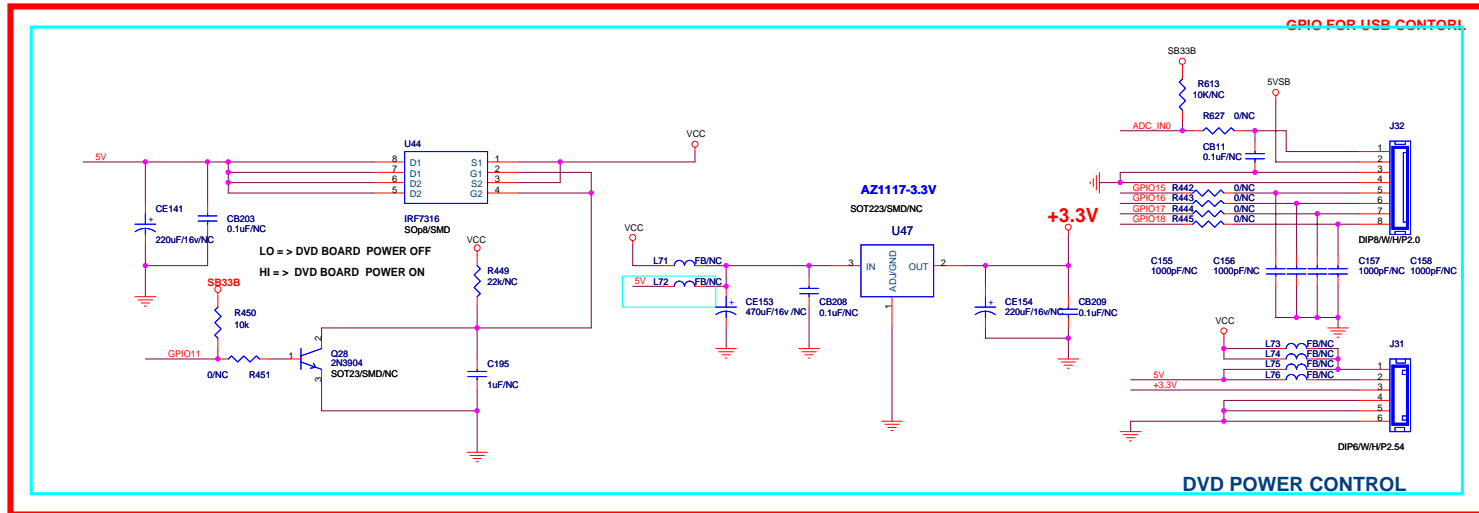
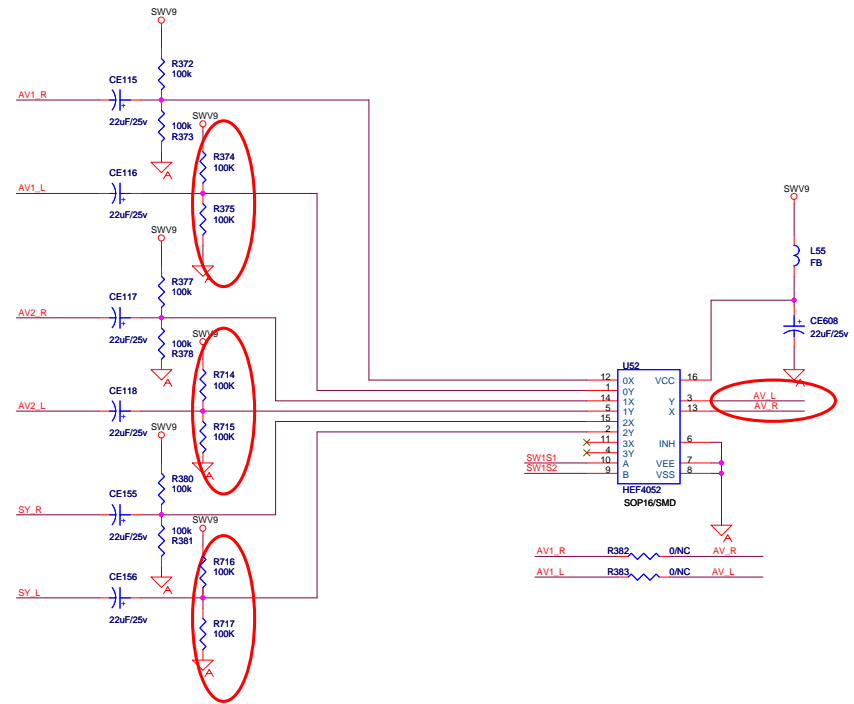
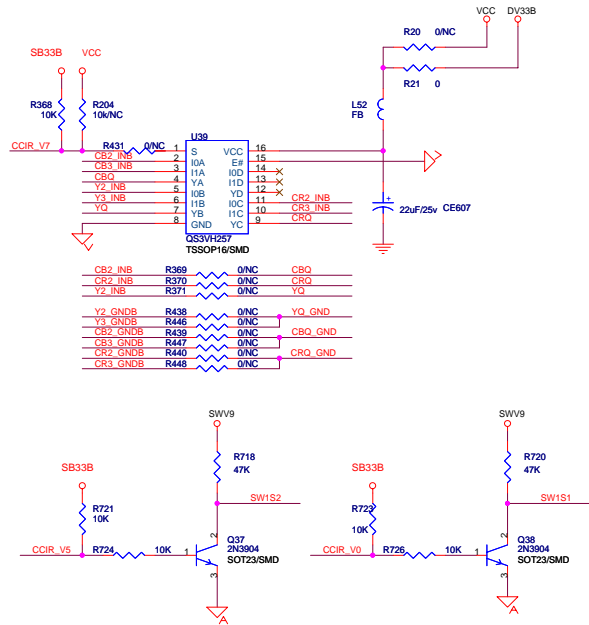
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INPUT

ADC_IN0	ADC_IN0	3
CCIR_V0	CCIR_V0	3
CCIR_V5	CCIR_V5	3
CCIR_V7	CCIR_V7	3
GPIO11	GPIO11	3
GPIO15	GPIO15	3
GPIO16	GPIO16	3
GPIO17	GPIO17	3
GPIO18	GPIO18	3
VFE_GND	VFE_GND	2,3,4,11
AADC_VSS	AADC_VSS	3,4,10
AV1_R	AV1_R	15
AV2_R	AV1_L	15
AV2_L	AV2_R	15
SV_R	AV2_L	15
SV_L	SV_R	15
YZ_INB	YZ_INB	15
YZ_GNDB	YZ_INB	15
CB2_INB	YZ_GNDB	10,15
CB2_GNDB	CB2_INB	15
CR2_INB	CB2_GNDB	10,15
CR2_GNDB	CR2_INB	15
Y3_INB	CR2_GNDB	10,15
Y3_GNDB	Y3_INB	15
CB3_INB	Y3_GNDB	15
CB3_GNDB	CB3_INB	15
CR3_INB	CB3_GNDB	15
CR3_GNDB	CR3_INB	15
SV	SV	1,7,9,14

OUTPUT

AV_R	AV_R	9
AV_L	AV_L	9
YQ	YQ	10
CBQ	CBQ	10
CRQ	CRQ	10
YQ_GND	YQ_GND	10
CBQ_GND	CBQ_GND	10
CRQ_GND	CRQ_GND	10



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CVBS0 >>> CVBS0 3
 CVBS1 >>> CVBS1 3
 CVBS2 >>> CVBS2 3

SY0 >>> SY0 3
 SC0 >>> SC0 3

SY1 >>> SY1 3
 SC1 >>> SC1 3

Y0+ >>> Y0+ 3
 Y0- >>> Y0- 3
 PB0+ >>> PB0+ 3
 PB0- >>> PB0- 3
 PR0+ >>> PR0+ 3
 PR0- >>> PR0- 3
 SOY0 >>> SOY0 3

Y1+ >>> Y1+ 3
 Y1- >>> Y1- 3
 PB1+ >>> PB1+ 3
 PB1- >>> PB1- 3
 PR1+ >>> PR1+ 3
 PR1- >>> PR1- 3
 SOY1 >>> SOY1 3

MPX1 >>> MPX1 3
 MPX2 >>> MPX2 3

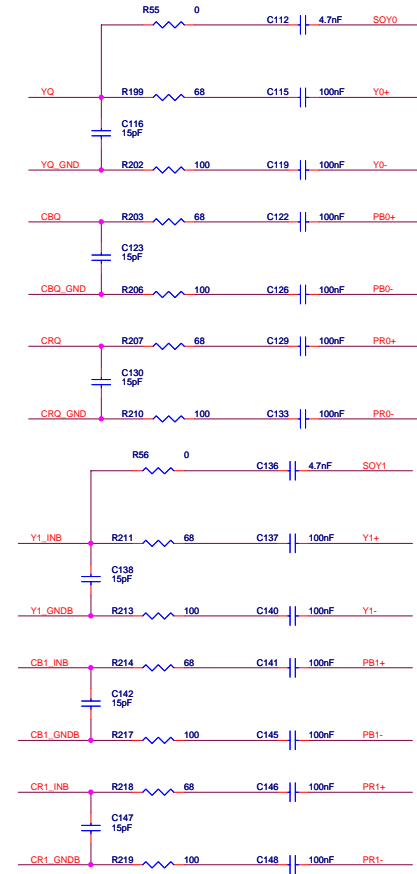
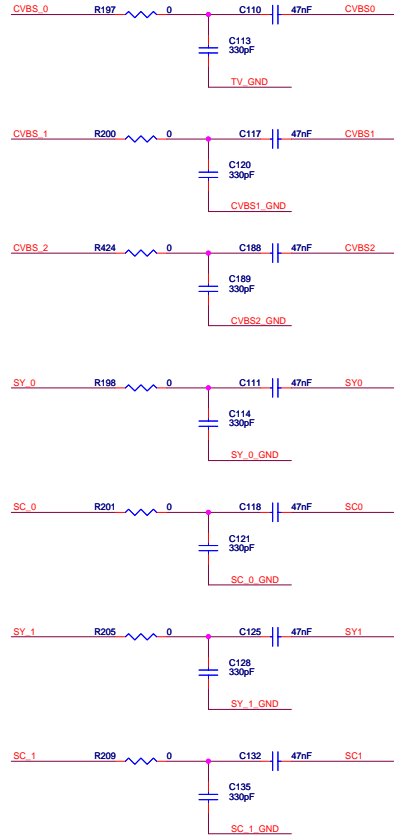
TO MT8202

TV_GND >>> TV_GND 14
 CVBS_0 >>> CVBS_0 14
 SIF >>> SIF 14
 AF >>> AF 14
 CVBS_1 >>> CVBS_1 15
 CVBS1_GND >>> CVBS1_GND 15
 CVBS_2 >>> CVBS_2 15
 CVBS2_GND >>> CVBS2_GND 15
 SY_1 >>> SY_1 15
 SY_1_GND >>> SY_1_GND 15
 SC_1 >>> SC_1 15
 SC_1_GND >>> SC_1_GND 15
 SY_0 >>> SY_0 15
 SY_0_GND >>> SY_0_GND 15
 SC_0 >>> SC_0 15
 SC_0_GND >>> SC_0_GND 15

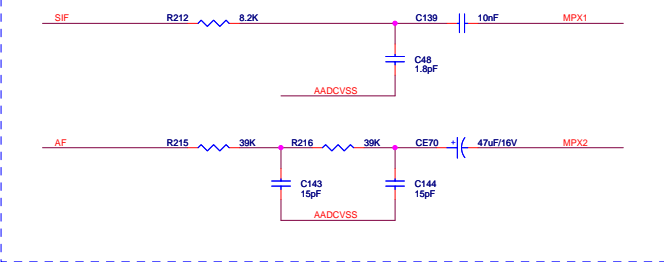
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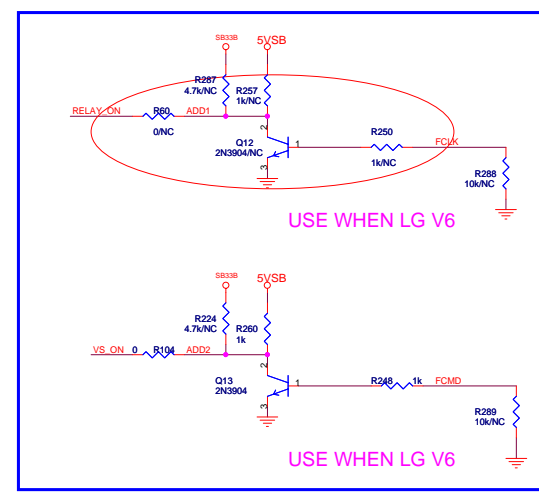
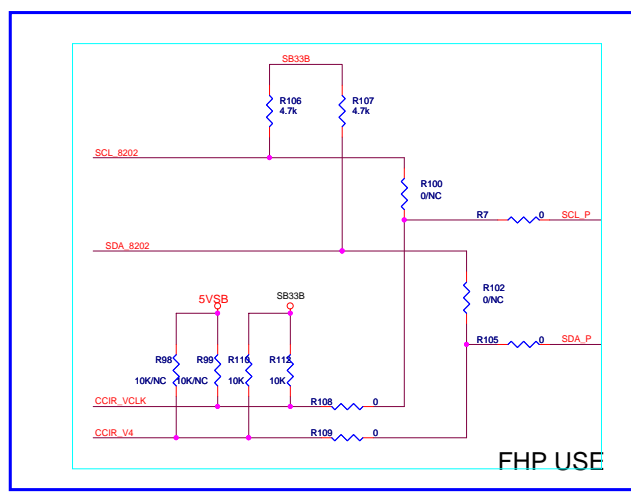
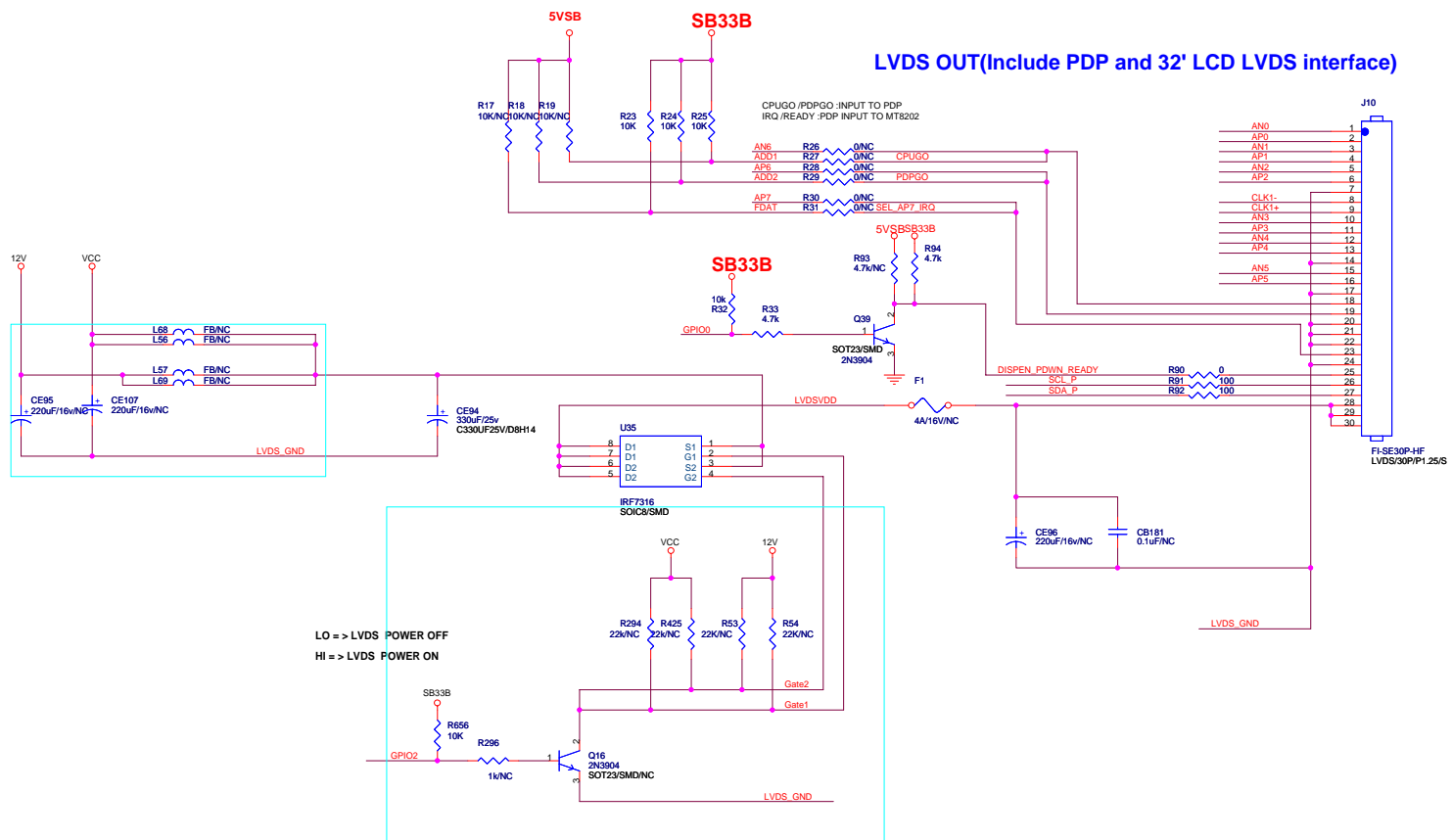
FROM Tuner



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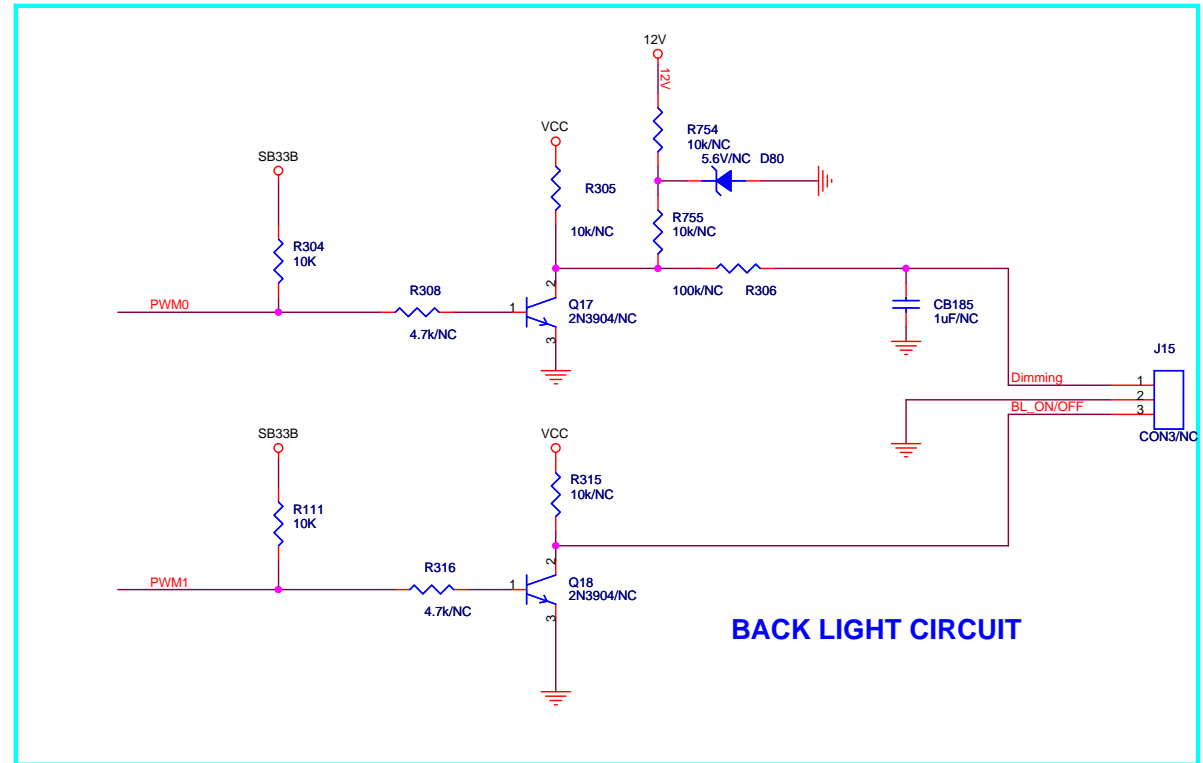
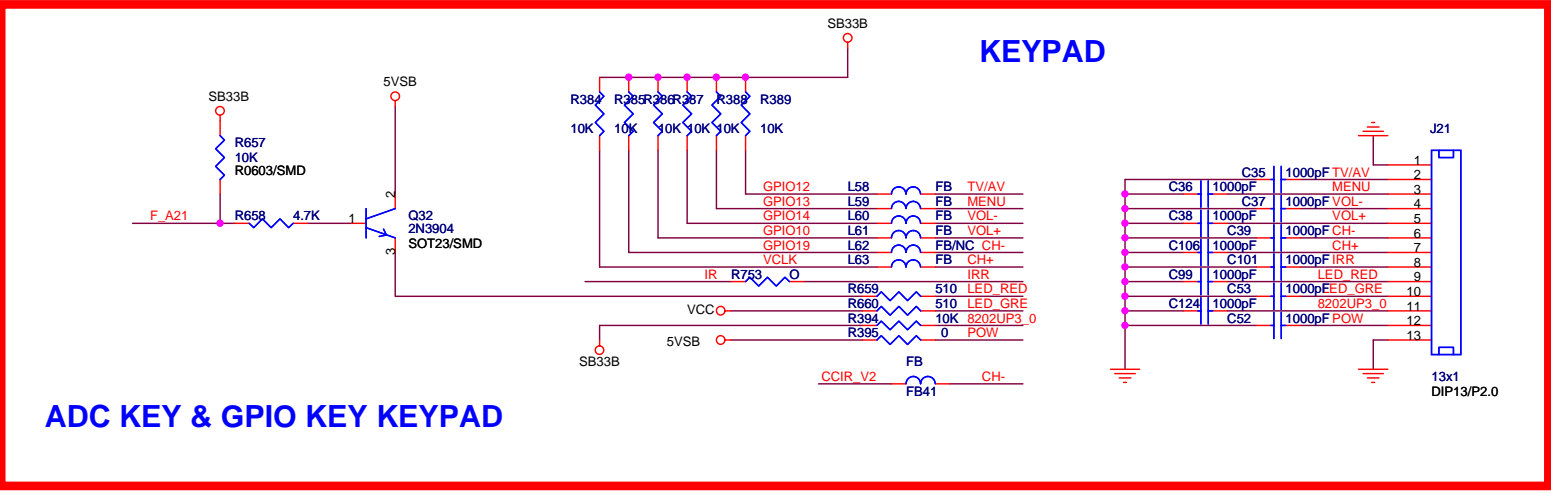
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GPIO2	>>	GPIO2	1,3
CLK1+	>>	CLK1+	3
CLK1-	>>	CLK1-	3
AP0_7	>>	AP0_7	3
AP0_6	>>	AP0_6	3
LVDS_GND	>>	LVDS_GND	2,3,4
LVDS1D0	>>	LVDS1D0	2,3,4
CCIR_VCLK	>>	CCIR_VCLK	3
CCIR_V4	>>	CCIR_V4	3
FCLK	>>	FCLK	3
FCMD	>>	FCMD	3
FDAT	>>	FDAT	3
SCL_8202	>>	SCL_8202	3,6,9
SDA_8202	>>	SDA_8202	3,6,9
RELAY_ON	>>	RELAY_ON	1
VS_ON	>>	VS_ON	1
12V	>>	12V	1,13



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LVDS OUT			
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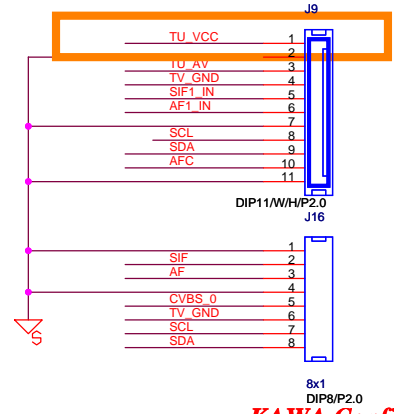
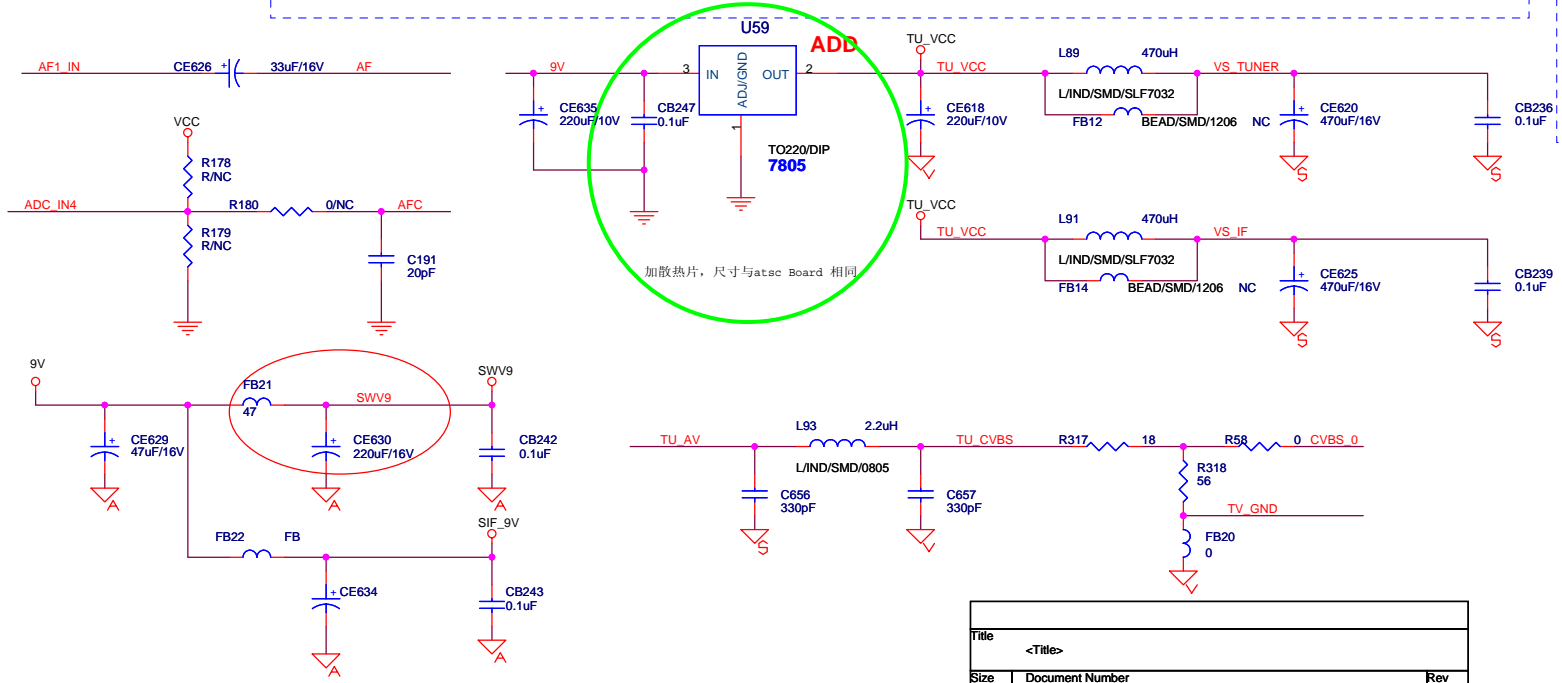
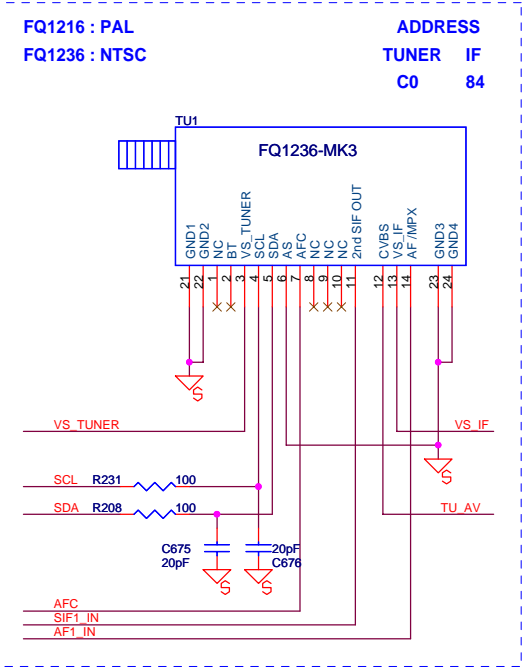
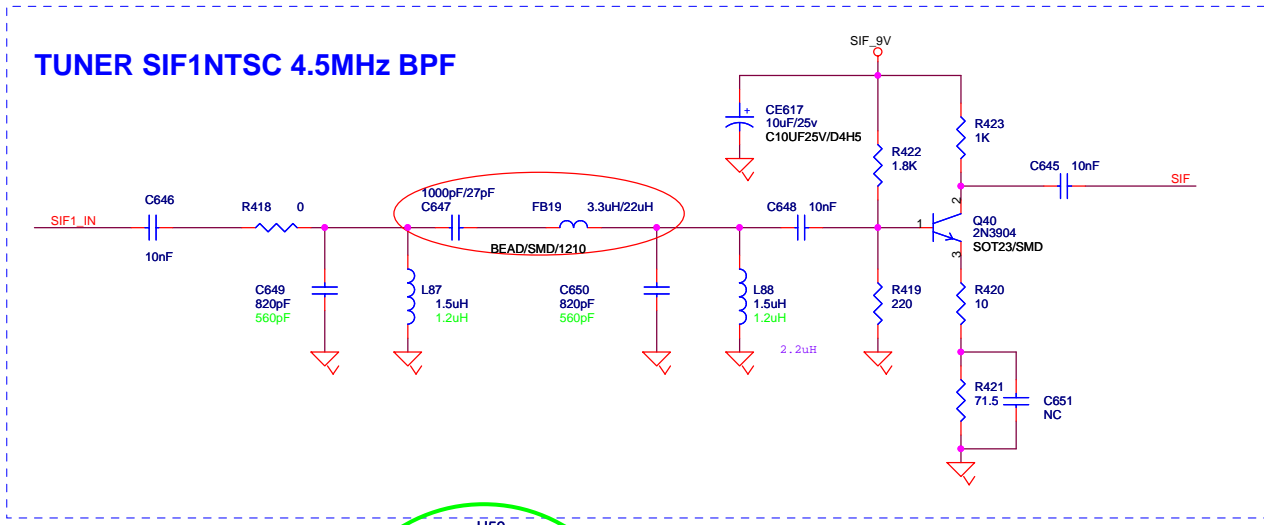
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GPIO10	>>>GPIO10	3
GPIO12	>>>GPIO12	3
GPIO13	>>>GPIO13	3
GPIO14	>>>GPIO14	1,3
PWM0	>>>PWM0	3
PWM1	>>>PWM1	3
8202UP3_0	>>>8202UP3_0	3
GPIO14	>>>GPIO14	1,3
GPIO19	>>>GPIO19	1,3
VCLK	>>>VCLK	3
F_A21	>>>F_A21	3
CCIR_V2	>>>CCIR_V2	3
12V	>>>12V	1,12



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BACK LIGHT / KEYPAD			
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SCL	SCL	1,9
SDA	SDA	1,9
CVBS_0	CVBS_0	10
TV_GND	TV_GND	10
AF	AF	10
SIF	SIF	10
ADC_IN4	ADC_IN4	3
9V	9V	1,7,9

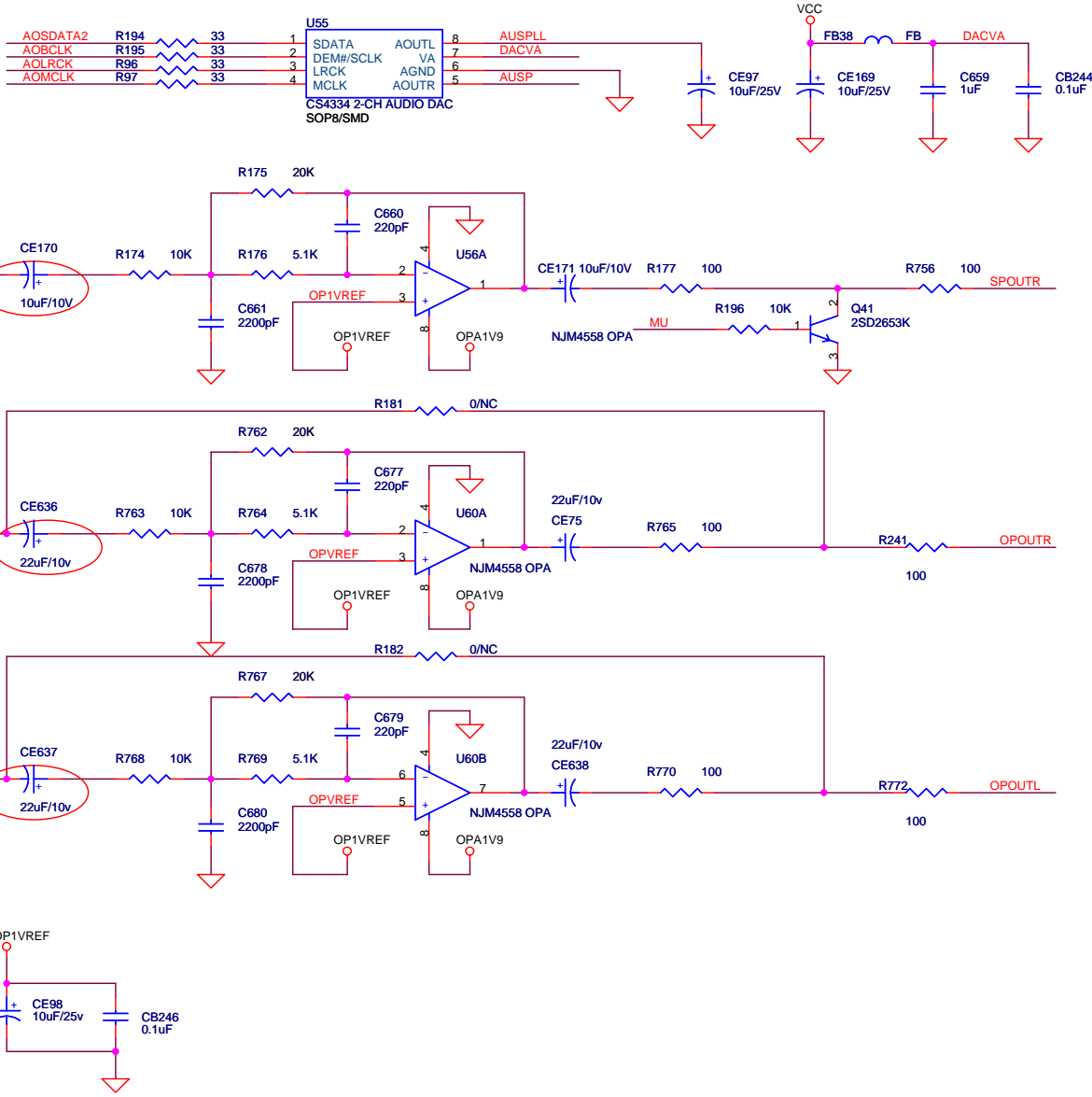


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AOSDATA2 >>> AOSDATA2 3
 AOMCLK >>> AOMCLK 3,9
 AOBCLK >>> AOBCLK 3,9
 AOLRCK >>> AOLRCK 3,9
 MU >>> MU 9
 SPOUTR >>> SPOUTR 15
 AUSPR >>> AUSPR 9
 AUSPL >>> AUSPL 9
 OPOUTL >>> OPOUTL 17
 OPOUTR >>> OPOUTR 17
 A_MUTE >>> A_MUTE 9,17



GPIO DECRPTION

- UP3_4 : SW SCL
- UP3_5 : SW SDA
- ERO0/UP3_0 :KEYPAD POWER
- ERO1/UP3_1 : MAIN POWER SWITCH
- VCLK : KEPAD CH+
- GPIO19 : KEPAD CH-
- DE/GPIO : DVD IR
- CCIR_CLK : PDP USE
- CCIR_V4 : PDP USE
- GPIO0 : PDP USE
- GPIO1 : NO USE
- GPIO2 : LVDS POWER SW
- GPIO3 : DTV POWER CONTROL
- GPIO4 : EEPROM WRITE PROTECT
- GPIO5/TXD : 2nd UART FOR MT5351
- GPIO6/RXD : 2nd UART FOR MT5351
- GPIO7 : AUDIO BYPASS MUTE CONTROL
- GPIO8 : SPEAKER SWITCH
- GPIO9 : AUDIO MUTE
- GPIO10 : Indicates active video at HDMI port
- GPIO11 : DVD POWER CONTROL
- GPIO12 : AV SWITCH
- GPIO13 : HDMI Hot Plug Detect
- GPIO14 : NO USE
- GPIO[15..18] : FOR DVD CONTROL
- GPIO/PWM0 : DIMMING
- GPIO/PWM1 : BACKLIGHT ON/OFF
- OUT_27Mhz/GPIO : HDMI CRYSTAL
- SDA1 : TO MT5351 I/F REQUEST
- SCL1 : TO MT5351 I/F READY
- F_A21 : KEYPAD(LED RED)
- ADCIN0 : KEYPAD
- ADCIN3:PDP 5VD DETECT
- ADCIN4:FOR TUNER AFC
- CCIR_V[0-3] : KEYPAD
- CCIR_V5 : AUDIO SWITCH
- CCIR_V6 : RESET DTV
- CCIR_V7 : YPBPR VIDEO SWITCH

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SUB WOOFER			
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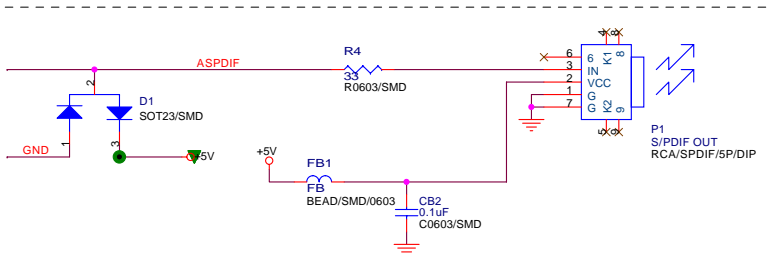
MT5111 / MT5351 REFERENCE DESIGN - 4 LAYERS

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RA-V1	INITIAL VERSION		2005/06/15
RA-V2	ADDED AUDIO SWITCH / REFINE POWER CIRCUIT		2005/07/14

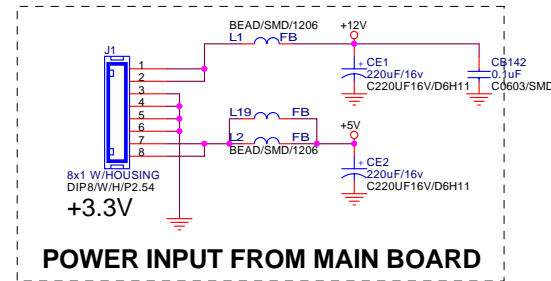
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- 02. POWER
- 03. TUNER
- 04. MT5111 ASIC
- 05. MT5351 ASIC
- 06. MT5351 PERIPHERAL
- 07. DDR MEMORY
- 08. NOR FLASH / JTAG / UART

NS : NON-STUFF

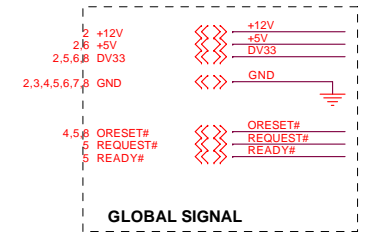
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+12V	POWER +12V	POWER SUPPLY
+5V	POWER +5V	POWER SUPPLY
+5V_tuner	POWER +5V	TUNER POWER
DV33_DM	POWER +3V3	MT5111 POWER
DV18	POWER +1V8	MT5111 POWER
DV33	POWER +3V3	MT5351 POWER
AV33	POWER +3V3	MT5351 ANALOG POWER
DV25	POWER +2V5	MT5351 DDR POWER
DV12	POWER +1V2	MT5351 POWER
GND	GROUND	GROUND



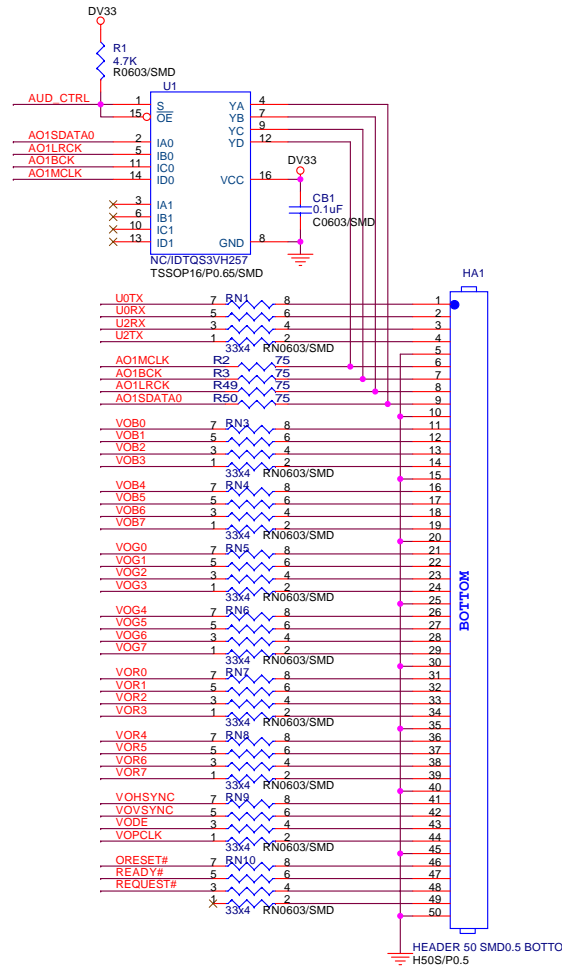
SPDIF CIRCUIT



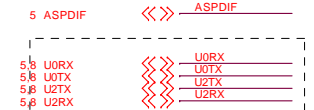
POWER INPUT FROM MAIN BOARD



GLOBAL SIGNAL



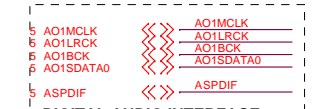
DIGITAL OUTPUT



UART (RS232)



DIGITAL VIDEO OUTPUT



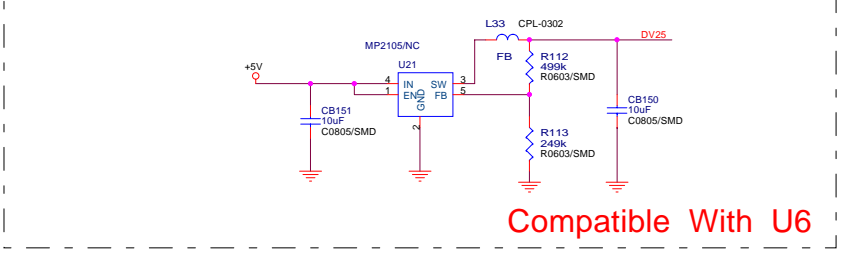
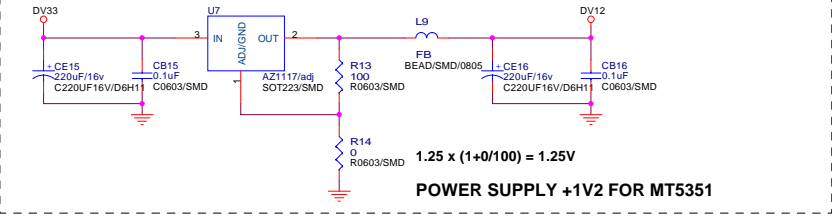
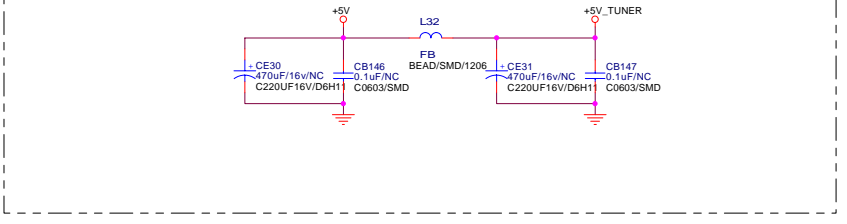
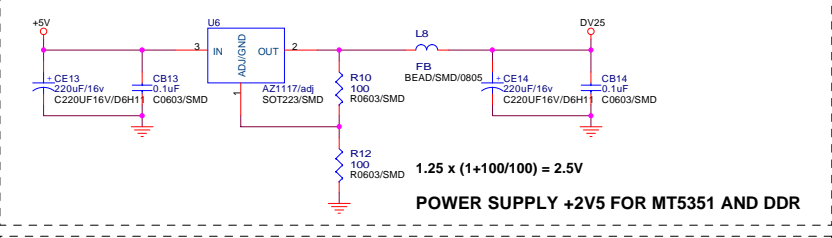
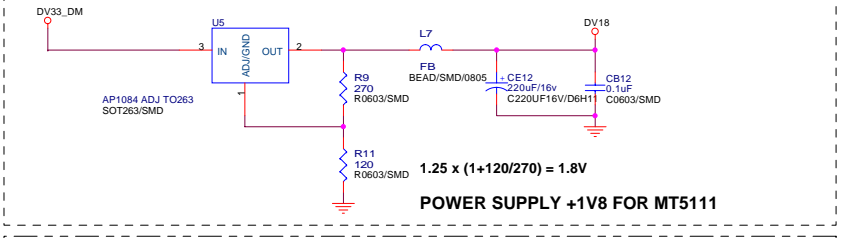
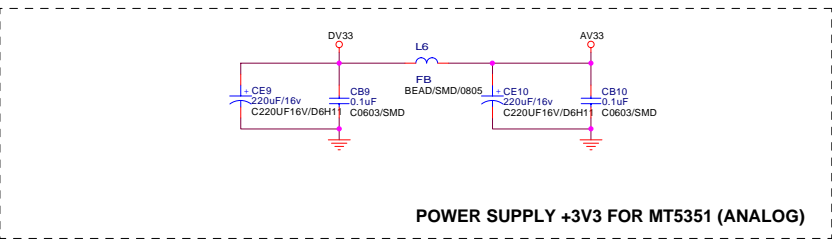
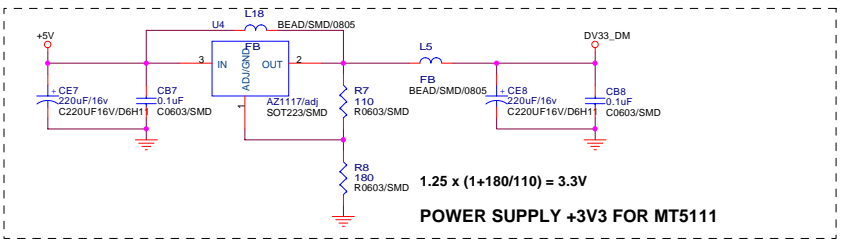
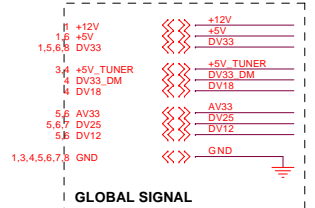
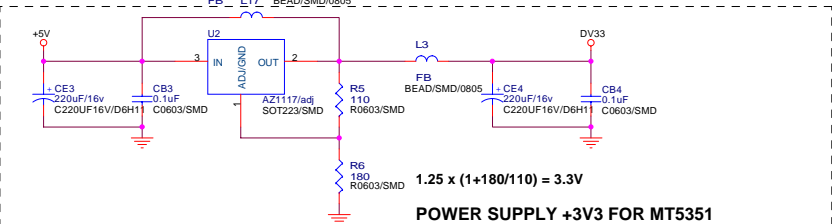
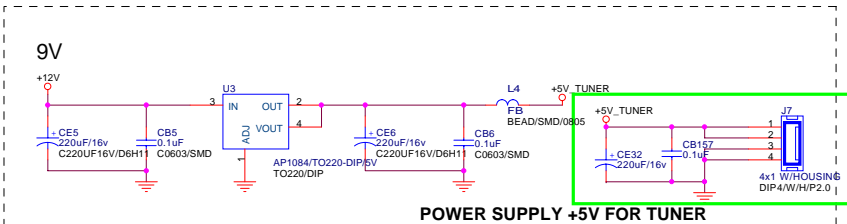
DIGITAL AUDIO INTERFACE



AUD_CTRL

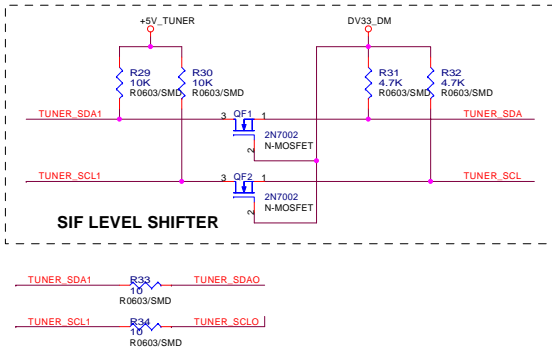
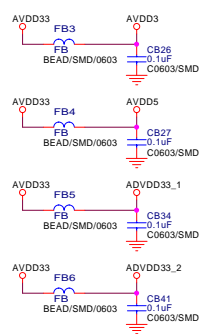
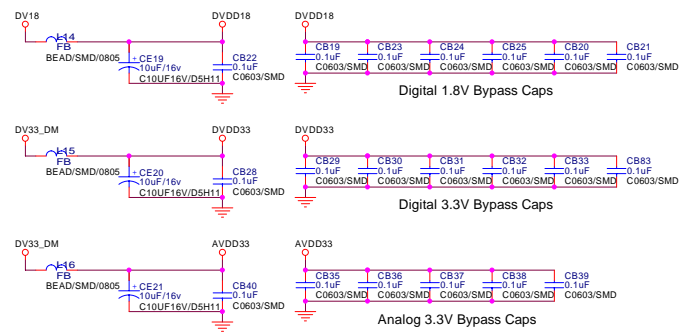
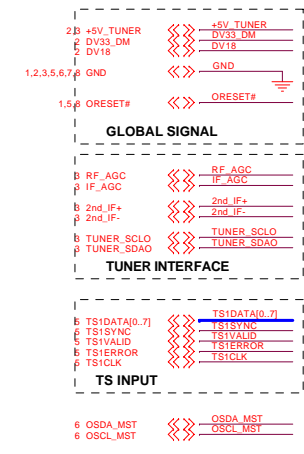
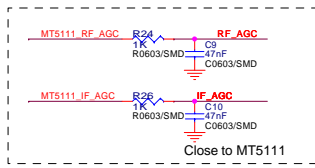
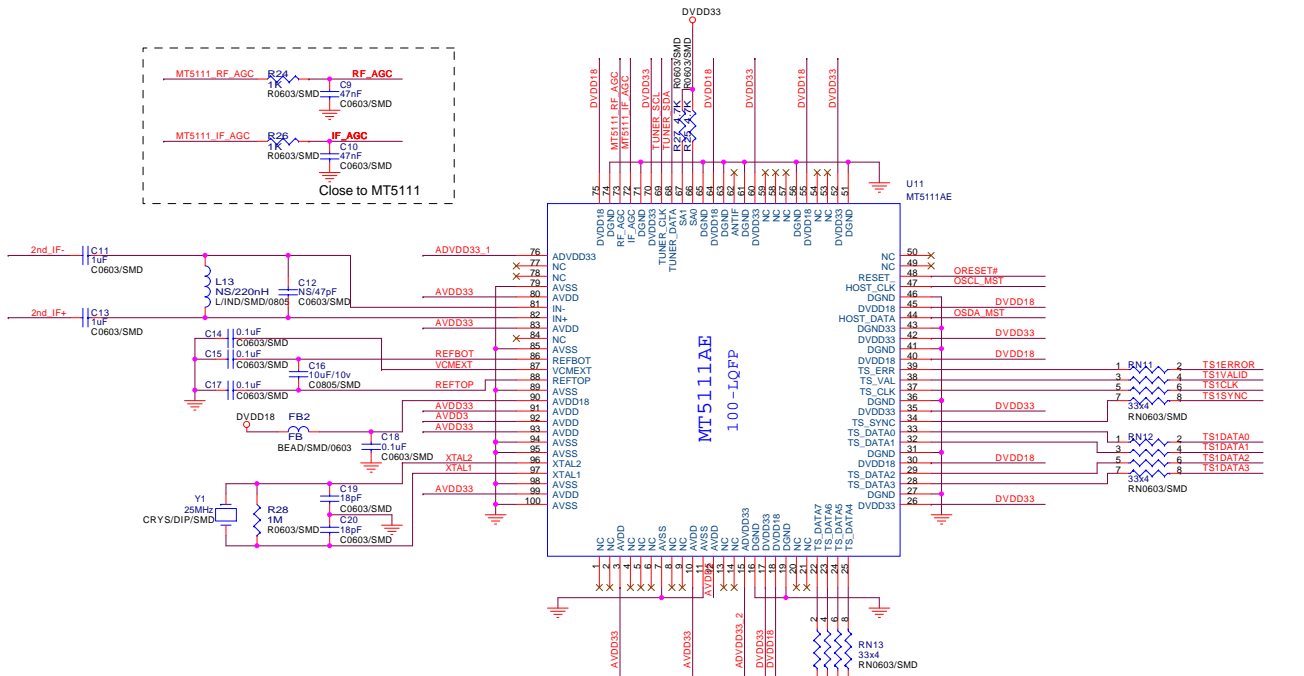
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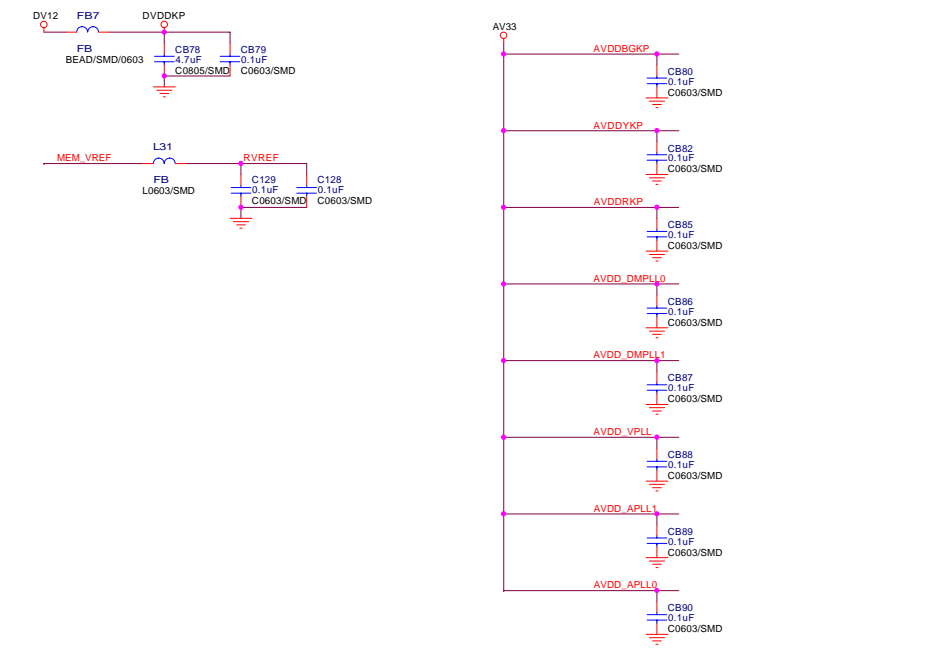
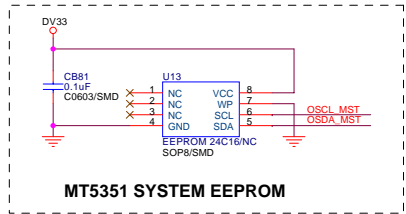
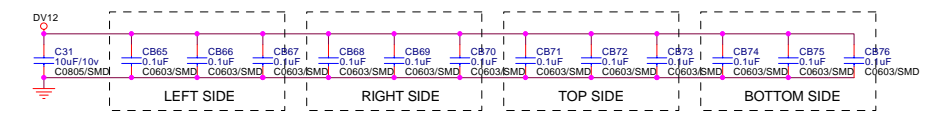
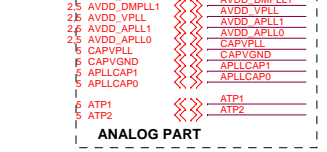
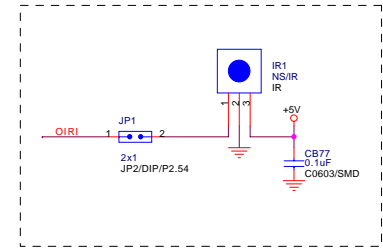
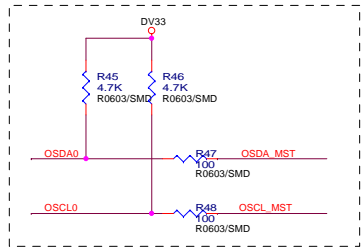
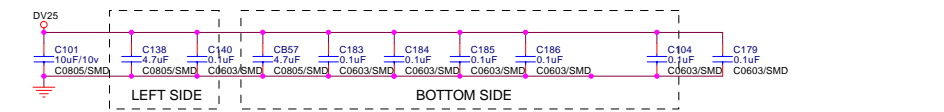
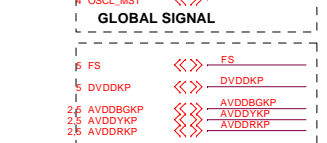
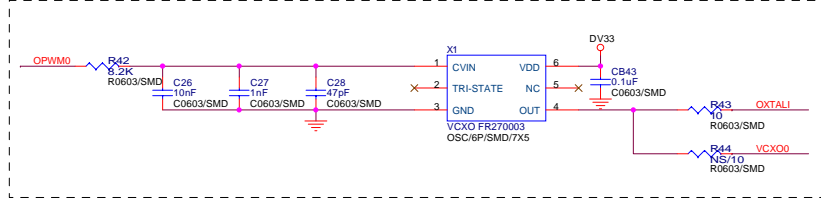
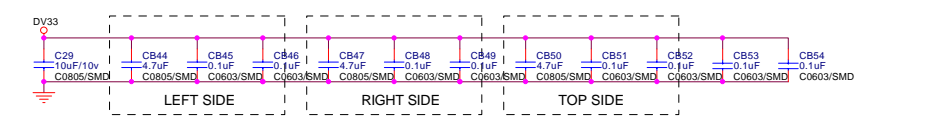
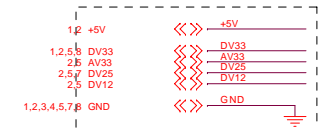
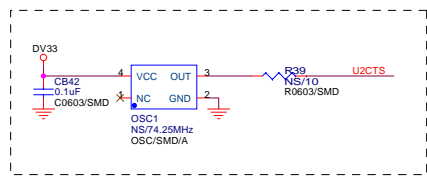
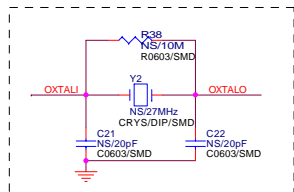
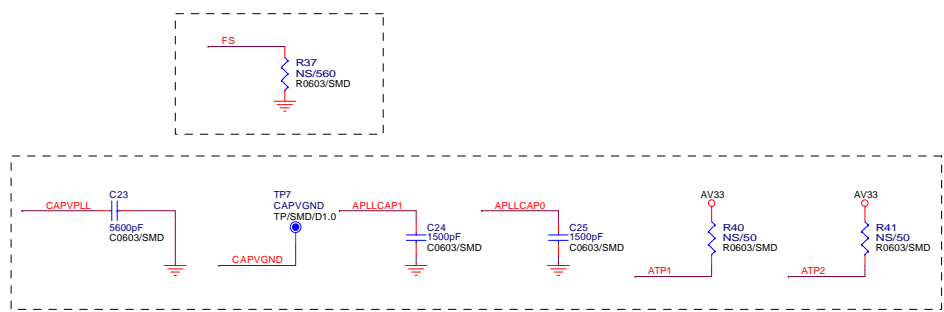
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Basic Operations & Circuit Description

MODULE

There are 1 pcs panel and 5 pcs PCB including 3 pcs Extension PCB, 1 pcs Timming controller board and 1 pcs Back Light board in the Module.

SET

There are 6 pcs PCBs including 1 pcs ATV Tuner board, 1 pcs keypad board, 1 pcs Remote Control Receiver board, 2 pcs L/R Speakers and 1 pcs Main(Video)board, 1 pcs ATSC board in the SET.

PCB funtion

1. Power :

(1). Input voltage: AC 120V, 60Hz.

(2). To provide power for PCBs.

2. Main board : To converter TV signals, S signals, AV signals, Y Pb/Cb Pr/Cr signals, DVI/HDMI signals and D-SUB signals to digital ones and to transmit to Control board.

3. Control board : Dealing with the digital signal for output to panel.

4. Extension board : Output addressing signals.

5. ATV Tuner Board : To convert TV RF signal to video and SIF audio signal to Main board.

6. ATSC Board : Receiver and converter ATSC TV signal to transmit to main board.

PCB failure analysis

1. CONTROL : a. Abnormal noise on screen. b. No picture.
2. MAIN :
 - a. Lacking color, Bad color scale.
 - b. No voice. (Make sure status: Mute / Internal, External speaker)
 - c. No picture but with signals output, OSD and back light.
 - d. Abnormal noise on screen.
3. POWER : NO picture, no power output.
4. Back Light :
 - a. No picture.
 - b. Flash on screen.
 - c. Darker picture with signals.
5. ATV Tuner :
 - a. No ATV Noise
 - b. No ATV signals
6. ATSC: a No ATSC TV signal

Main IC Specifications

- M13S128168A (ESMT)
2M x 16 Bit x 4 Banks Double Data Rate SDRAM
- MT5111CE
Single-Chip HDTV/CATV Demodulator
- MT8206
- MT8293
HDMI PanelLink Cinema Receiver
- R2S15102NP
Digital Power Amplifier R2S15102NP
- WM8776
24-bit, 192kHz Stereo CODEC with 5 Channel I/P Multiplexer

MT5111CE

Single-Chip HDTV/CATV Demodulator

Key Features

- Compliant with ATSC digital television standard
- Supports SCTE DVS-031 and ITU J.83 Annex B digital CATV standard
- Accepts direct IF (44 MHz or 43.75MHz) and low IF (5.38MHz)
- Differential IF input with programmable input signal level: 0.5Vpp to 2Vpp
- NTSC interference rejection capability
- Compensate echo up to -5 to +47us range for terrestrial HDTV reception
- On-chip 10-bit ADC for HDTV/CATV demodulator
- On-chip programmable gain amplifier
- 25MHz crystal for clock generation
- On-chip PLL clock generation
- Full-digital timing recovery, no VCXO is required
- Full-digital frequency offset recovery with wide acquisition range ± 1 MHz for ATSC and ± 250 KHz for CATV reception
- Dual digital AGC controls for IF and RF respectively
- MPEG-2 transport stream output in parallel or serial format
- On-chip error rate estimators for TS packets, TCM decoder, and equalizer
- EIA/CEA-909 antenna interface
- Controlled by I²C interface
- Supports sleep mode to save power consumption
- Core power supply: 1.8V, peripheral power supply: 3.3V
- 100-LQFP package
- Lead Free

Functional Block Diagram

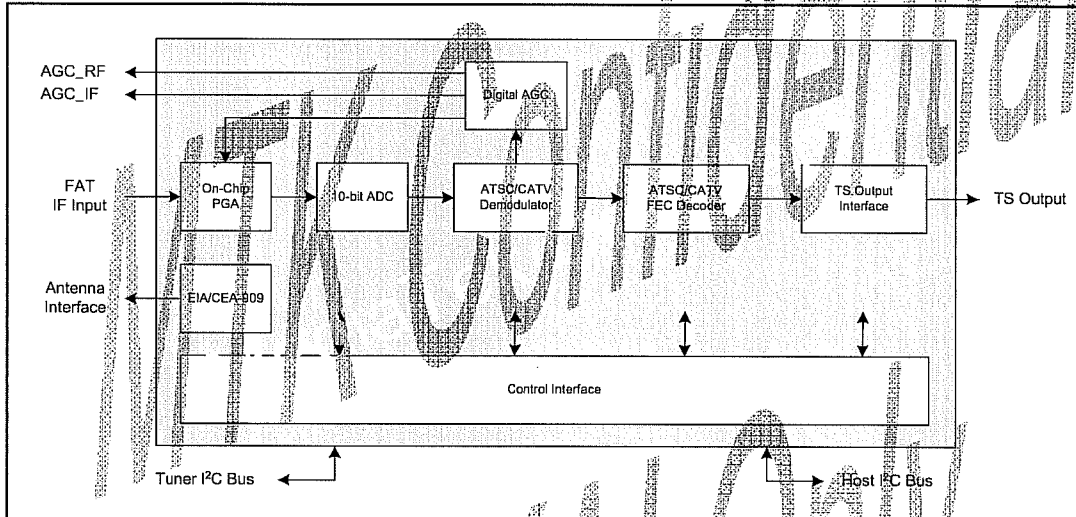


Figure 1: MT5111CE Functional Block Diagram

General Description

MT5111CE is a fully integrated single-chip 8-VSB and 64/256-QAM demodulator. The chip is designed specifically for the digital terrestrial HDTV and CATV receivers, and is fully compliant with ATSC A/53, SCTE DVS-031, and ITU J.83 Annex B standards.

MT5111CE includes a 10-bit A/D converter, 8-VSB/QAM demodulator, TCM (Trellis-Coded Modulation) decoder, and Reed-Solomon Forward Error Correction decoder. Moreover, an internal controller handles the acquisition and tracking to ensure the best receiving performance. The internal controller communicates with the external host controller via the I2C-compatible interface, and also provides direct control to the RF tuner via the second I2C-compatible

interface.

MT5111CE accepts either the direct IF signals centered at 44MHz or 43.75MHz, or the low IF signals centered at 5.38MHz. The center frequency of the incoming IF signal can also be programmed to other frequencies for various applications. An On-chip programmable gain-controlled amplifier is designed to provide sufficient signal amplitude when the received RF signal is weak. The IF signal is first sampled by a 10-bit A/D converter. Afterward, the digitized samples are further processed for adjacent channel interference rejection.

MT5111CE measures the power level of the digitized sequence, and feeds the control voltages back to the RF tuner and the IF amplifier respectively. The control voltages are converted to analog signals through the on-chip 1-bit sigma-delta D/A converters plus the off-chip R-C low-pass filters. The automatic gain control keeps the received power level at a desired level and maximizes the received SNR.

The carrier frequency offset and symbol timing offset are both estimated and compensated by a fully digital synchronizer. The synchronizer also controls the rate conversion in the digital re-sampling device by estimating the sampling frequency offset. All synchronization in MT5111CE are integrated in digital circuits, no external VCXO is required.

The equalizer is adopted to cancel the effect of multi-path fading channel during signal propagation in the air or over cable networks. The equalizer is not only capable of acquiring correct coefficients combination by specified adaptive algorithms, but also programmable to different configurations for various channel conditions.

The following FEC decoder corrects most of the errors by the concatenation

of TCM and Reed-Solomon decoders. For CATV reception, MT5111CE detects and aligns de-puncturing timing of the received sequence. The timing synchronization is also automatically performed to lock the FEC frames. The on-chip error rate estimator can simultaneously monitor the receiving qualities at the three stages: equalizer output, TCM decoder, and transport stream packets. The chip finally outputs the decoded MPEG-2 packets in either the serial or parallel transport stream format.

In addition to the demodulation of HDTV signal, MT5111CE also provides the capability to remove the NTSC co-channel interference. To achieve the best reception condition, an antenna interface compliant with EIA/CEA-909 is designed to control the antenna parameters.

MT5111CE is designed with efficient mechanisms of power saving. When configured to enter the sleep mode by the system host, it can immediately turn off almost all embedded hardware except the on-chip controller to reduce the power consumption. Resuming from sleep mode is also triggered by the system host. Upon returning to the operation mode, the chip will try to re-acquire the DTV signal automatically.

Pin Out

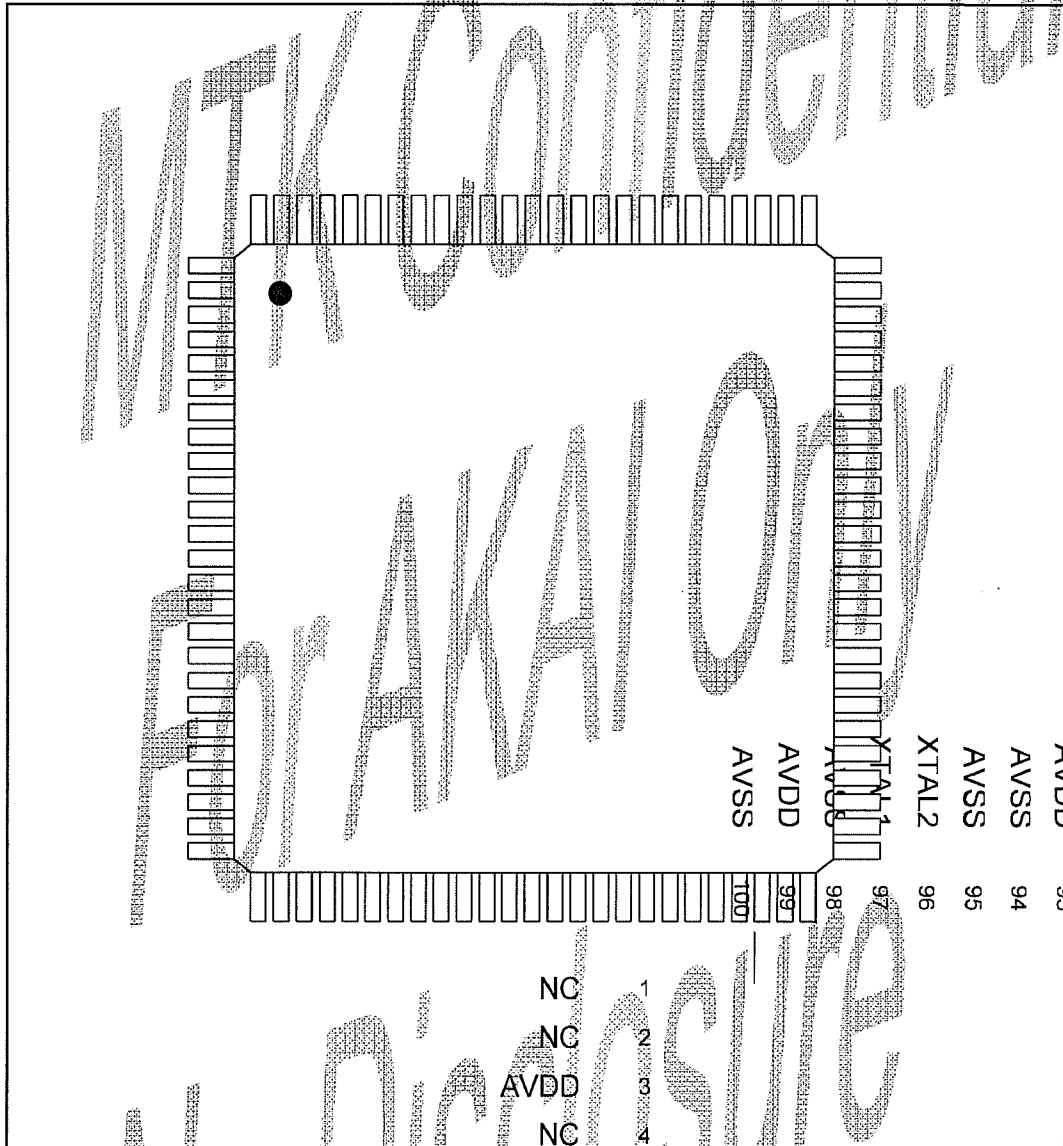


Figure 2. MT5111CE Pin Out

AVSS	7
NC	8
NC	9
AVDD	10
AVSS	11
AVDD	12
NC	13
NC	14
ADVDD3.3	15

Pin Description

Signal Name	Pin No	I/O	Description
Transport Stream			
TSDATA[7:0]	22,23,24,25,28, 29,32,33	O	TS data output
TSSYNC	34	O	TS packet start signal
TSVAL	38	O	TS output valid signal
TSCLK	37	O	TS output clock
TSERR	39	O	TS packet error indicator
Analog Signal			
IN+	82	I	Analog differential IF input
IN-	81	I	
REFTOP	88	O	ADC reference top voltage. Decouple with a capacitor to AVSS
REFBOT	86	O	ADC reference bottom voltage. Decouple with a capacitor to AVSS
VCMEXT	87	O	ADC common mode voltage
Antenna Interface			
ANTIF	62	O	CEA-909 Antenna Control Interface
Clock Generation			
XTAL1	97	I	25MHz crystal input
XTAL2	96	I	
Control Signals			
HOST_CLK	47	I	Host processor serial clock input, 5 volt compatible
HOST_DATA	44	I/O	Host processor serial data pin, 5 volt compatible
TUNER_CLK	69	O	Tuner serial clock output, 5 volt compatible
TUNER_DATA	68	I/O	Tuner serial data pin, 5 volt compatible
IF_AGC	72	O	IF AGC output
RF_AGC	73	O	RF AGC output
RESET	48	I	Power reset pin, low active
SA0	66	I	Chip slave address selection pin, tie to VDD3.3 or DGND
SA1	67	I	Chip slave address selection pin, tie to VDD3.3 or DGND
Power Supply			
VDD3.3	17,26,35,42, 52,60,70	P	Digital power supply, tie to 3.3V
VDD1.8	18,30,40,45, 55,64,75	P	Digital power supply, tie to 1.8V
DGND	16,19,27,31, 36,41,43,46,51,56, 61,63,65,71,74	P	Digital ground, tie to digital ground plane
AVDD	3,10,12,80,83,91, 92,93,99	P	Analog power supply, tie to 3.3V
AVSS	7,11,79,85,89,94, 95,98,100	P	Analog ground, tie to analog ground plane
ADVDD3.3	15,76	P	Digital power supply for analog component, tie to 3.3V
AVDD1.8	90	P	Digital power supply for analog component, tie to 1.8V
Others			
NC	1,2,4,5,6,8,9,13,14, 20,21,49,50,53,54, 57,58,59,77,78,84		Not Connected

Table 1: Pin Description

Electrical Characteristic

Recommended Operating Condition

Symbol	Description	Min	Typical	Max	Unit
T _j	Chip Junction Temperature	-	-	125	°C
VDD1.8	1.8V Digital Core Power Supply Voltage	1.62	1.8	1.98	Volt
AVDD	3.3V Analog Power Supply Voltage	3.15	3.3	3.45	Volt
VDD3.3	3.3V Digital IO Power Supply Voltage	3	3.3	3.6	Volt
AVDD1.8	1.8V Analog Power Supply Voltage	1.7	1.8	1.9	Volt
V _{IH}	Digital Input High Voltage	3	3.3	3.6	Volt
V _{IL}	Digital Input Low Voltage	-	0	-	Volt

Table 2: Recommend Operating Condition

Typical Current and Power Dissipation (ASTC Mode)

Symbol	Description	Typical	Unit
I_VDD1.8	1.8V Digital Core Power Supply Current	350	mA
I_AVDD	3.3V Analog Power Supply Current	70	mA
I_VDD3.3	3.3V Digital I/O Power Supply Current	16	mA
I_AVDD1.8	1.8V Analog Power Supply Current	2	mA
P_VDD1.8	1.8V Digital Core Power Dissipation	630	mW
P_AVDD	3.3V Analog Power Dissipation	231	mW
P_VDD3.3	3.3V Digital IO Power Dissipation	52.8	mW
P_AVDD1.8	1.8V Analog Power Dissipation	3.6	mW
P_Total	Total Power Dissipation	917.4	mW
P_Sleep	Total Power Dissipation (Sleep Mode)	130	mW

Table 3: Typical Current and Power Dissipation (ATSC Mode)

Typical Current and Power Dissipation (QAM Mode)

Symbol	Description	Typical	Unit
I_VDD1.8	1.8V Digital Core Power Supply Current	175	mA
I_AVDD	3.3V Analog Power Supply Current	70	mA
I_VDD3.3	3.3V Digital I/O Power Supply Current	19	mA
I_AVDD1.8	1.8V Analog Power Supply Current	2	mA
P_VDD1.8	1.8V Digital Core Power Dissipation	315	mW
P_AVDD	3.3V Analog Power Dissipation	231	mW
P_VDD3.3	3.3V Digital I/O Power Dissipation	62.7	mW
P_AVDD1.8	1.8V Analog Power Dissipation	3.6	mW
P_Total	Total Power Dissipation	612.3	mW
P_Sleep	Total Power Dissipation (Sleep Mode)	130	mW

Table 4: Typical Current and Power Dissipation (QAM Mode)

MT8206 is a highly integrated single chip for LCD TV supporting video input and output format up to HDTV. It includes 3D comb filter TV decoder to retrieve the best image from popular composite signals. Embedded HDTV/VGA decoders enable the high quality video reproduction. 24/16/8 bits digital port may accept all kinds of external digital input video source. New 3rd generation advanced motion adaptive de-interlacer converts accordingly the interlace video into progressive non-flicking video. 2D Graphic engine generates high quality UI interface. Advanced full function color processing with fully 10-bit path provides high quality video contents. Independent two Flexible scalars provide wide adoption to various LCD panels for two of different video sources at the same time. Its on-chip audio processor decodes analog signals from tuner with lip sync control, delivering high quality post-processed sound effect to customers. On-chip microprocessor reduces the system BOM and shortens the schedule of UI design by high level C program. MT8206 is a cost-effective and high performance HDTV-ready solution to LCD TV product.

FEATURES

- Video Input
 - Support fully programmable 8 Composite/SV input pins
 - Support 2 Component inputs with SDTV format & HDTV 480i/576i/480p/576p/720p/1080i /1080p format
 - Support VGA input up to SXGA (1280x1024x75Hz) including SOG signals
 - Support Digital 24-bit RGB and CCIR 656/601 24/16/8 bit digital input
 - Support Fully Scart function
- TV decoder
 - Full 10-bit data path to enhance the video resolution and reduce digital truncation errors
 - Support PAL (B, G, D, H, M, N, I, Nc), PAL (Nc), PAL, NTSC, NTSC-4.43, SECAM
 - Automatic Luma/Chroma gain control
 - Automatic TV standard detection
 - The 3rd generation NTSC/PAL Motion Adaptive 3D comb filter with huge improvement
 - VBI decoder for Closed-Caption/XDS/Teletext/WSS/VPS
 - High speed advanced Teletext/Closed-Caption drawing engine directly on OSD plane
 - Macrovision detection
- Video Processor
 - Fully 10-bit processing to enhance the video quality
 - Advanced flesh tone and color processing
 - Gamma/anti-Gamma correction
 - Advanced Color Transient Improvement (CTI)
 - 2D Peaking
 - Advanced horizontal/vertical sharpness
 - Saturation/hue/contrast/Brightness adjustment
 - Black level extender
 - White peak level limiter
 - Adaptive Luma/Chroma management
 - Automatic detect film or video source
 - 3:2/2:2 pull down source detection
 - 3rd generation Advanced Motion adaptive de-interlacing
 - The 3rd generation Advanced 2D/3D Noise reduction for all video paths
 - Arbitrary ratio vertical/horizontal scaling of video, from 1/32X to 32X
 - Advanced linear and non-linear Panorama scaling
 - Programmable Zoom viewer
 - Progressive scan output
 - Picture-in-Picture (PIP)
 - Picture-Out-Picture (POP)
 - Advanced dithering processing for LCD display with 6/8/10 bit output
 - Frame rate conversion, 50Hz to 75Hz
- Audio DSP
 - Support BTSC/EIAJ/A2/NICAM decode
 - Stereo demodulation, SAP demodulation
 - Noise reduction
 - Mode selection (Main/SAP/Stereo)
 - Pink noise and white noise generator
 - Equalizer
 - Sub-woofer/Bass enhancement
 - Noise auto mute
 - 3D surround processing include virtual surround
 - Audio and video lip synchronization
 - Support Reverberation
- Audio Input/Output
 - Decode audio AF from Tuner
 - 2 channel audio L/R digital line in
 - 7.1-channel slave digital line in
 - Including full 7.1-channels digital output, 2-channel bypass and 2-channel headphone output
 - Embedded 3 internal DAC output
 - Support 2 independent Audio outputs

■ DRAM Controller

- Supports up to 32M-byte SDR/DDR DRAM
- Supports 2x16 bit SDR/DDR bus interfaces
- Build in a DRAM interface programmable clock to optimize the DRAM performance
- Programmable DRAM access cycle and refresh cycle timings
- Maximum DRAM clock rate is 175MHz
- Support 3.3/2.5-Volt SDR/DDR Interface

■ Video Output

- Embedded TV pattern generator
- Interlaced 50Hz to 120Hz
- Support up to 1080P resolution
- Dual-channel 6/8/10-bit LVDS output
- Support video output mirror and upside down

■ 2D-Graphic/3 OSD processor

- Embedded Two backend RGB domain OSD planes and one YUV domain OSD
- Support Text/Bitmap decoder
- Support line/rectangle/gradient fill
- Support bitblt
- Support color Key function
- Support Clip Mask
- Support Alpha blending with video output

- 65535/256/16/4/2-color bitmap format OSD,
- Automatic vertical scrolling of OSD image
- Support OSD mirror and upside down

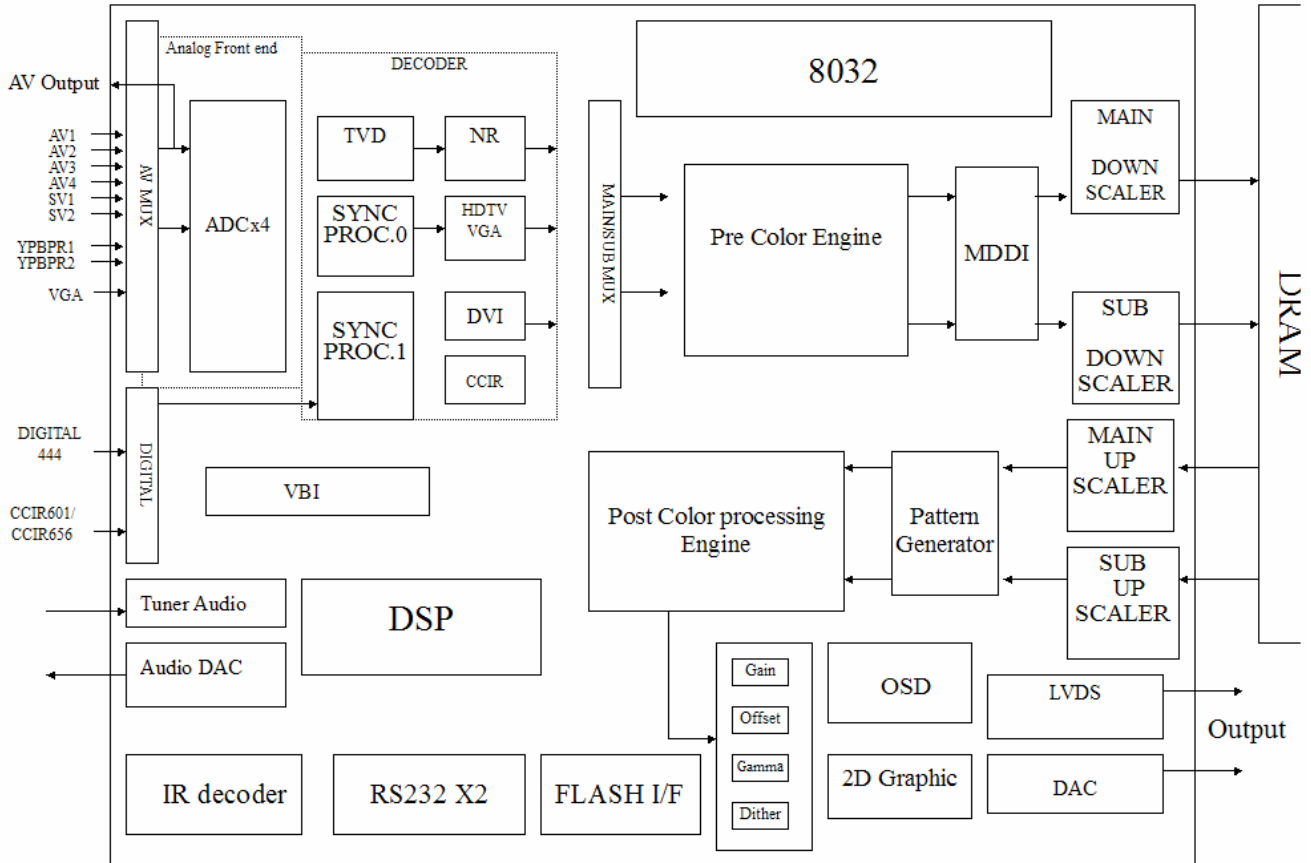
■ Host Micro controller

- Turbo 8032 micro controller
- Built-in internal 373 and 8-bit programmable lower address port
- 2048-bytes on-chip RAM
- Up to 4M bytes FLASH-programming interface
- Supports 5/3.3-Volt. FLASH interface
- Supports power-saving mode
- Supports additional serial port
- IR control serial input
- Support dual RS232 interfaces for external source interface
- Support 2 PWMs output
- Support DDC2Bi
- Programmable GPIOs setting for complex external device control

■ Outline

- 388-pin BGA package
- 3.3/1.8-Volt. Dual operating voltages
- 0.18um process

BLOCK DIGRAM



Analog Switch

Analog switches are built in MT8206 to connect to 17 input signals and there is need to add external components to add analog video multiplexes on board.

There are 9 high-speed differential input pairs for 3 sets of YPRPB/VGA input signals.

The 8 Composite/S signal input pins can be fully programmed to connect to any AV/SV inputs.

ADC/ Source Select

The video ADC sample analog input signals. After ADC, all signal processing is digital domain. The source select multiplex all inputs from digital and analog video ports and route them into data path.

Audio Interface

Audio interface accept analog audio signal from Tuner, e.g. AF. It also includes preprocessing circuit to filter the noisy audio signals. Audio decoder will decode the BTSC or NICAM, and output best sound with enhanced 3D surround post-processing.

Embedded 7.1 channel digital audio input (slave) and 2 channels (master) digital audio inputs.

Embedded 3 high performance audio DACs.

DSP

DSP handle audio decoding as well as computing intensive jobs. The downloadable micro code enables fast function convergence for various audio standards in the world.

Advanced DSP engine supports full functions of sound effects.

Support Dolby Surround and WOW SRS

MDDi/Scaler

MDDi is MTK proprietary de-interlacing technology. The 3rd generation MDDi solution provides improved low angle processing and more accurate motion detection for all interlace sources. The techniques reduce jagged edges and broken images. The MDDi engine supports both Main and Sub channel SDTV inputs or one channel 1080i high quality de-interlacing.

Two totally independent scalers support full functions of PIP/POP and frame rate conversion.

With MDDi and high quality scaler, MT8206 guarantee all input format could be translated to output format with best video quality for motion and still pictures.

Color/Gamma

MT8206 provides advanced color management engine for user to improve video quality with fully flexibility. With contrast/hue/saturation/Gamma/anti-Gamma/flesh tone function, and well algorithm control, MT8206 deliver the best video quality with vivid color.

Advanced dither function support 6/8/10-bit video output for any kinds of display unit (LCD, PDP, CRT).

8032

On-chip Turbo8032 provide the most cost effective development environment for system house. Well-proven F/W could speed up the system design significantly.

2D-G/OSD

On-chip graphic engine draw bitmap OSD and store them into DRAM. OSD read data from DRAM and display on screen. With 2D-G and OSD. The computing power requirement of μ P will be minimized.



MTK

MT8293

Specifications are subject to change without notice.

HDMI PanelLink Cinema Receiver

MT8293 is a low-cost, fully HDMI-compliant receiver that fits directly into home theater products such as LCD TVs, plasma TVs and HDTVs. The receiver is capable of supporting bandwidths up to 165MHz and video resolutions up to 1080p and UXGA. The MT8293 supports the DVD-Audio standard, including 7.1- surround audio at 96kHz and stereo audio at 192kHz.

The built-in High-bandwidth Digital Content Protection (HDCP) decryption engine secures the digital link for transmission of valuable high-definition video and audio. Built-in HDCP self-test engine simplifies manufacturing testing.

FEATHRES

■ Industry-Standard

- HDMI 1.1
- DVI 1.0
- EIA/CEA-861B
- HDCP 1.1

■ Digital Video Output

- Integrated PanelLink Core
- Supports DTV (480i/576i/480p/576p/720p/1080i/1080p) and PC (VGA/XGA/SXGA/UXGA) resolution up to 165MHz (using dual edge to transmit video data for pixel clock over 112MHz)
- Flexible digital video interface
 - 24-bit RGB/YCbCr 4:4:4
 - 16-bit YCbCr 4:2:2
 - 8-bit YCbCr 4:2:2 (ITU-R BT.656)
- Integrated RGB <-> YCbCr color space conversion (both 601 and 709)
- 4:2:2 <-> 4:4:4 converter
- Integrated Deinterlacer for 480i/576i (SDTV only)
- Integrated Down-Scaler (with CEN)

■ Digital Audio Output

- Industry-standard S/PDIF and 3-wire output

- Supports high-end audio including DVD-Audio
 - 2-ch. 32-192kHz or
 - 8-ch. 32-96kHz
- Programmable 3-wire output supports numerous low-cost I2S audio DACs
- Supports IEC60958 2-channel PCM
- Capable of carrying IEC61937 compressed audio (Dolby Digital, DTS, etc.)

■ Content Protection

- Integrated HDCP cipher engine
- External EEPROM for encrypt HDCP keys
- Built-in HDCP self-test
- Decrypts both video and audio

■ System Operation

- Register-programmable via slave I2C interface
- Auto video mode
- Auto audio mode
- Flexible interrupt registers with interrupt pin

■ Power Management

- 1.8V core provides low-power operation
- Flexible power-down modes

■ Outline

- 128-pin QFP package



MT8293

PRELIMINARY, SUBJECT TO CHANGE WITHOUT NOTICE

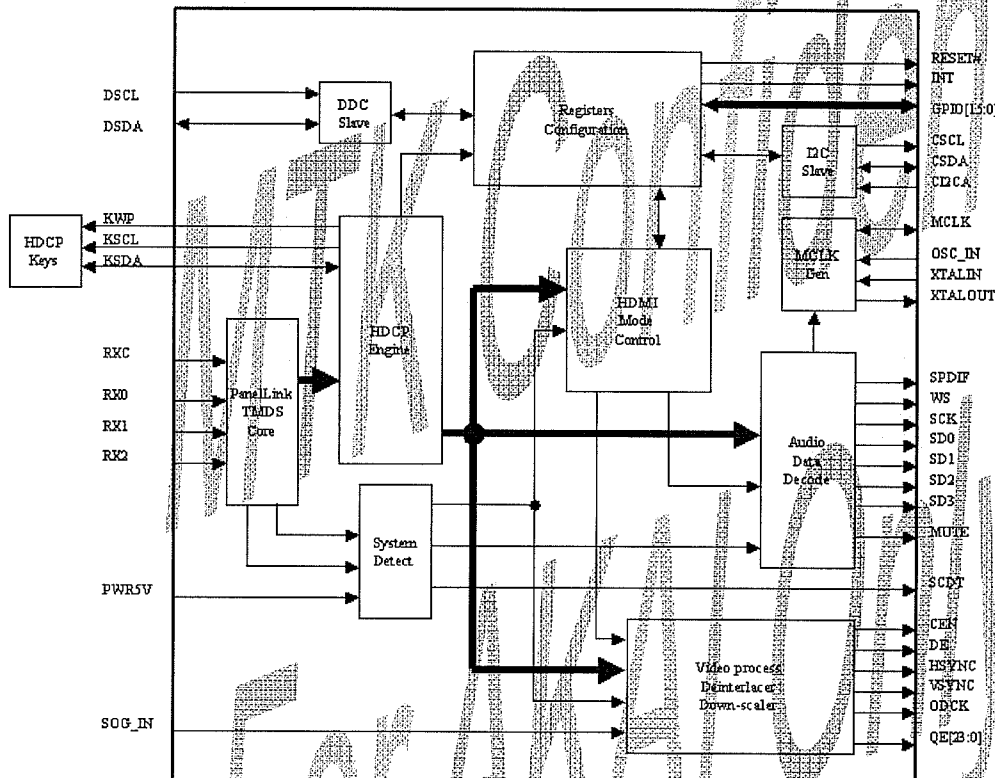
MTK CONFIDENTIAL, NO DISCLOSURE

CGND18	85	32	GP103
CVCC18	86	31	IOVCC33
MUTE	87	30	IOGND33
IOVCC33	88	29	GP104
IOGND33	89	28	GP105
SPDIF	70	27	GP106
SD3	71	26	GP107
SD2	72	25	CGND18
SD1	73	24	CVCC18
SD0	74	23	GP108
WS	75	22	GP109
SCK	76	21	GP110
IOVCC33	77	20	GP111
IOGND33	78	19	IOVCC33
MCLK	79	18	IOGND33
CGND18	80	17	GP112
CVCC18	81	16	GP113
AUXP_VCC18	82	15	GP114
AUXPGND	83	14	GP115
XTALOUT	84	13	CGND18
XTALIN	85	12	CVCC18
XTALVCC	86	11	KSCL
REGVCC	87	10	NSDA
RSVDL	88	9	KMP
RESET#	89	8	NC
SCDT	90	7	IOVCC33
INT	91	6	IOGND33
QE23	92	5	NC
QE22	93	4	OSC_IN
QE21	94	3	SOG_IN
QE20	95	2	CEN
QE19	96	1	VSYN
		126	HSYNC
		127	DE
		128	CGND18
		125	CVCC18
		124	DE
		123	DE
		122	DE
		121	DE
		120	IOVCC33
		119	IOVCC33
		118	IOGND33
		117	IOGND33
		116	DE
		115	DE
		114	DE
		113	CGND18
		112	CGND18
		111	DE
		110	DE
		109	DE
		108	DE
		107	IOVCC33
		106	IOVCC33
		105	IOGND33
		104	IOGND33
		103	DE
		102	DE
		101	DE
		100	DE
		99	DE
		98	IOVCC33
		97	IOGND33



MT8293

No Disclosure



FOR ANALYSIS ONLY

NO DISCLOSURE

Item	Symbol	Pin #	Type	Description
DIGITAL				
Power/Ground (45)				
1	CVCC18	12,24,36,45,66,81,112,125	I	Digital Logic 1.8V power
2	CGND18	13,25,37,65,80,113,126	I	Digital Logic ground
3	IOVCC33	7,19,31,68,77,98,107,120	I	Input/Output Pin 3.3V power
4	IOGND33	6,18,30,69,78,97,106,118	I	Input/Output Pin ground
5	AVCC	49,53,57,61	I	TMDS Analog 3.3V power
6	AGND	52,56,60,64	I	TMDS Analog ground
7	PVCC	47	I	TMDS PLL 3.3V power
8	PGND	46	I	TMDS PLL ground
9	AUDPVCC18	82	I	ACR PLL 1.8V power
10	AUDPGND	83	I	ACR PLL ground
11	XTALVCC	86	I	ACR PLL crystal input 3.3V power
12	REGVCC	87	I	ACR PLL regulator 3.3V power
Configuration/Programming (20)				
1	INT	91	O	Interrupt output
2	RESET#	89	I	Reset Pin. Active low
3	DSCL	42	I	DDC I2C clock, 5V tolerance
4	DSDA	41	I/O	DDC I2C data, 5V tolerance
5	CSCL	40	I	Configuration I2C clock
6	CSDA	39	I/O	Configuration I2C data
7	KSCL	11	O	KEYS EEPROM I2C clock
8	KSDA	10	I/O	KEYS EEPROM I2C data
9	KWP	9	O	KEYS EEPROM write protect
10	SCDT	90	O	Indicates active video at HDMI input port
11	CISCA	38	I	I2C device address select

Item	Symbol	Pin #	Type	Description
12	PWR5V	44	I	TMDS port transmitter detect (hot plug), 5V tolerance
13	RSVDL	88	I	Must be tied low
14	RSVD	48	O	
15	NC	43	-	No connect
16	NC	8,5	-	No connect
17	OSC_IN	4	I	Oscillator input, External in
18	SOG_IN	3	I	SOG input, External AD in
19	CEN	2	O	Clock enable, for 8202 CEN input
Digital Audio Interface (9)				
1	MCLK	79	I/O	Audio master clock input reference
2	SCK	76	O	I2S serial clock output
3	WS	75	O	I2S word select output
4	SD0	74	O	I2S serial data output
5	SD1	73	O	I2S serial data output
6	SD2	72	O	I2S serial data output
7	SD3	71	O	I2S serial data output
8	SPDIF	70	O	S/PDIF audio output
9	MUTE	67	O	Mute audio output
GPIO Interface (16)				
1	GPIO0	35	I/O	GPIO
2	GPIO1	34	I/O	GPIO
3	GPIO2	33	I/O	GPIO

Item	Symbol	Pin #	Type	Description
4	GPIO3	32	I/O	GPIO
5	GPIO4	29	I/O	GPIO
6	GPIO5	28	I/O	GPIO
7	GPIO6	27	I/O	GPIO
8	GPIO7	26	I/O	GPIO
9	GPIO8	23	I/O	GPIO
10	GPIO9	22	I/O	GPIO
11	GPIO10	21	I/O	GPIO
12	GPIO11	20	I/O	GPIO
13	GPIO12	17	I/O	GPIO
14	GPIO13	16	I/O	GPIO
15	GPIO14	15	I/O	GPIO
16	GPIO15	14	I/O	GPIO
TTL Interface (28)				
1	DE	127	O	Data enable
2	VSYNC	1	O	Vertical sync
3	HSYNC	128	O	Horizontal sync
4	ODCK	119	O	Output data clock
5	QE0	124	O	24-bit Even pixel
6	QE1	123	O	24-bit Even pixel
7	QE2	122	O	24-bit Even pixel

Item	Symbol	Pin #	Type	Description
8	QE3	121	O	24-bit Even pixel
9	QE4	117	O	24-bit Even pixel
10	QE5	116	O	24-bit Even pixel
11	QE6	115	O	24-bit Even pixel
12	QE7	114	O	24-bit Even pixel
13	QE8	111	O	24-bit Even pixel
14	QE9	110	O	24-bit Even pixel
15	QE10	109	O	24-bit Even pixel
16	QE11	108	O	24-bit Even pixel
17	QE12	105	O	24-bit Even pixel
18	QE13	104	O	24-bit Even pixel
19	QE14	103	O	24-bit Even pixel
20	QE15	102	O	24-bit Even pixel
21	QE16	101	O	24-bit Even pixel
22	QE17	100	O	24-bit Even pixel
23	QE18	99	O	24-bit Even pixel
24	QE19	96	O	24-bit Even pixel
25	QE20	95	O	24-bit Even pixel
26	QE21	9	O	24-bit Even pixel
27	QE22	93	O	24-bit Even pixel
28	QE23	92	O	24-bit Even pixel



Item	Symbol	Pin #	Type	Description
ANALOG (8)				
Differential signal				
1	RXC+	51	I	TMDS input clock pair
1	RXC-	50	I	TMDS input clock pair
1	RX0	55	I	TMDS input data pair
1	RX0	54	I	TMDS input data pair
1	RX1	59	I	TMDS input data pair
1	RX1	58	I	TMDS input data pair
1	RX2	63	I	TMDS input data pair
1	RX2	62	I	TMDS input data pair
PLL group(2)				
68	XTALIN	85	I	Crystal input PAD
69	XTALOUT	84	O	Crystal output PAD

No Disclosure



MTK

MT5351

Specifications are subject to change without notice.

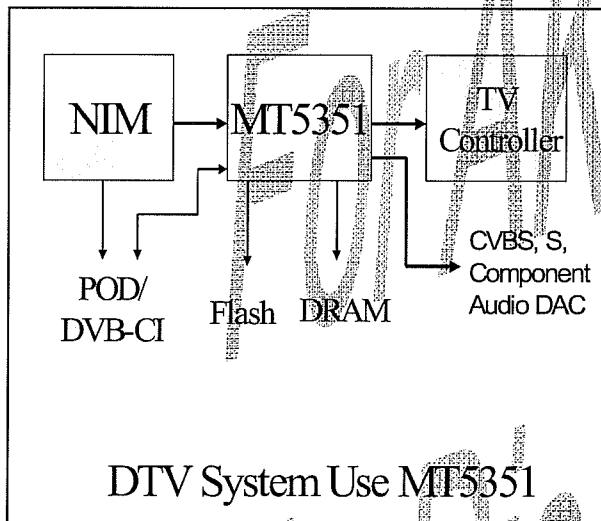
DTV Backend Decoder SOC

MediaTek MT5351 is a DTV Backend Decoder SOC which support flexible transport demux, HD MPEG-2 video decoder, JPEG decoder, MPEG1,2, MP3, AC3 audio decoder, HD TV encoder. The MT5351 enables consumer electronics manufacturers to build high quality, feature-rich DTV, STB or other home entertainment audio/video device.

World-Leading Technology: HW support worldwide major broadcast network and CA standards, include ATSC, DVB, OpenCable, DirectTV, MHP.

Rich Feature for high value product: To enrich the feature of DTV, the MT5351 support 1394-5C component to external DVHS. Dual display, PIP/POP and quad pictures provide user a whole new viewing experience.

Credible Audio/Video Quality: The MT5351 use advanced motion-adaptive de-interlace algorithm to achieve the best movie/video playback. The embedded 4X over-sample video DAC could generate very fine display quality. Also, the audio 3D surround and equalizer provide professional entertainment



Key Features:

1. Flexible Demuxer
2. Dual HD MPEG2 Video Decoder
3. Dual MPEG1,2, MP3, AC3 Audio decode
4. Dual Display
5. PIP/POP/Quad Mode
6. IEEE1394-5C
7. POD/DVB-CI

Application:

1. DTV
2. Set-top Box
3. DTV Recorder
4. Home Media Center

Order Information:

MT5351AG → one HD decoder
 MT5351CG → two HD decoder
 All Package are Lead Free

M **ARM**
 MT5351AG
 DDDD-B#L
 LLLLL

IC Top View:

DDDD: Date Code
 #: Subcontractor Code
 LLLLL: Lot Number

General Feature List

- Host CPU
 - ARM 926EJ
 - 16K I-Cache and 16K D-Cache
 - 8K Data TCM and 8K Instruction TCM
 - JTAG ICE interface
 - Watch Dog timers
- Transport Demuxer
 - Support 3 independent transport stream inputs
 - Support serial / parallel interface for each transport stream input.
 - Support ATSC, DVB, and MPEG2 transport stream inputs
 - Programmable sync detection.
 - Support DES/3-DES de-scramble
 - 96 PID filter and 128 section filters.
 - Support TS recording via IEEE1394 interface
- MPEG2 Decoder
 - Support dual MPEG-2 HD decoder or up to 8 SD decoder
 - Complaint to MP@ML, MP@HL and MPEG-1 video standards
- JPEG Decoder
 - Decode Base-line or progressive JPEG file
- 2D Graphics
 - Support multiple color modes
 - Point, horizontal/vertical line primitive drawing
 - Rectangle fill and gradient fill functions
 - Bitblt with transparent, alpha blending, alpha composition and stretch
 - Font rendering by color expansion
 - Support clip masks
 - YCbCr to RGB color space transfer
- OSD Display
 - 3 linking list OSDs with multiple color mode
 - OSD scaling with arbitrary ratio from 1/2x to 2x
 - Square size, 32x32 or 64x64 pixel, hardware cursor
- Video Processing
 - Advanced Motion adaptive de-interlace on SDTV resolution
 - Support clip
 - 3:2:2:2 pull down; source detection
 - Arbitrary ratio vertical/horizontal scaling of video, from 1/15X to 16X
 - Support Edge preserve
 - Support horizontal edge enhancement
 - Support Quad-Picture
- Main Display
 - Mixing two video and three OSD and hardware cursor
 - Contrast/Brightness adjustment
 - Gamma correction
 - Picture-in-Picture (PIP)
 - Picture-Out Picture (POP)
 - 480i/576i/480p/576p/720p/1080i output
- Auxiliary Display
 - Mixing one video and one OSD
 - 480i/576i output
- TV Encoder
 - Support NTSC M/N, PAL M/N/B/D/G/H/I
 - Macrovision Rev 7.1.L1
 - CGMS/WSS
 - Closed Captioning
 - Six 12-bit video DACs for CVBS, S-video or RGB/YPbPr output
- Digital Video Interface
 - Support SA/EAV
 - Support 8/16 for SD/HD digital video input
 - Support 8/16/24 bits digital output for main display
 - Support 8 bits digital output for aux display
- DRAM Controller
 - Supports 64Mb to 1Gb DDR DRAM devices
 - Configurable 32/64 bit data bus interface
 - Support DDR266, DDR333, DDR400 JEDEC specification compliant SDRAM
- Peripheral Bus Interface
 - Support NOR/NAND flash
 - Support CableCard host control bus
- Audio

- Support Dolby Digital AC-3 decoding
 - MPEG-1 layer I/II, MP3 decoding
 - Dolby prologic II
 - Main audio output: 5.1ch + 2ch (down mix)
 - Auxiliary audio output: 2ch
 - Pink noise and white noise generator
 - Equalizer
 - Bass management
 - 3D surround processing include virtual surround
 - Audio and video lip synchronization
 - Support reverberation
 - SPDIF out
 - I2S I/F
- Peripherals
- Three UARTs with Tx and Rx FIFO, two of them have hardware flow control
 - Two serial interfaces, one is master only, the other can be set to master mode or slave mode
 - Two PWMs
 - IR blaster and receiver
 - IEEE 1394 link controller
 - IDE bus: ATA/ATAPI7 UDMA mode 5, 100 MB/s
 - Real-time clock and watchdog controller
 - Memory card I/F: MS/MS-Pro, SD, CF, and MMC
 - PCMCIA/POD/CI interface
- IC Outline
- 471 Pin BGA Package
 - 3.3V/1.2V dual Voltage

Electrical Characteristics

Absolute Maximum Rating

Symbol	Parameters	Value	Unit
IOVDD	3.3V supply voltage	-0.5 to 4.6	V
CVDD	1.2V supply voltage	-0.5 to 1.8	V
AVDD	Analog supply voltage	-0.5 to 4.6	V
RVDD	DDR supply voltage	-0.5 to 3.5	V
VIN(3.3V)	Input Voltage(3.3V IO)	VSS-1.0 to 3.63	V
VIN(5V tolerance)	Input Voltage(5V tolerance IO)	VSS-1.0 to 5.5	V
Vout	Output Voltage	-0.3 to VDD3+0.3	V
Ts	Storage Temperature	-40 to 150	C
Ta	Ambient Temperature	0 to 70	C

DC Characteristics

Symbol	Parameters	Min	Typ	Max	Unit
IOVDD	3.3V supply voltage	2.97	3.3	3.63	V
CVDD	1.2V supply voltage	1.08	1.2	1.32	V
AVDD	Analog supply voltage	2.97	3.3	3.63	V
VIH(3.3V)	3.3V input voltage high	2.0			V
VIL(3.3V)	3.3V input voltage low			0.8	V
VOH(3.3V)	3.3V output voltage high	2.4			
VOL(3.3V)	3.3V output voltage low			0.4	
VIH(3/5V)	3/5V tolerance input voltage high	2.0			V
VIL(3/5V)	3/5V tolerance input voltage low			0.8	V
VOH(3/5V)	3/5V tolerance output voltage high	2.4			V
VOL(3/5V)	3/5V tolerance output voltage low			0.4	V
Tj	Junction operation temperature	-40	25	125	C
PD(estimate)	Power dissipation		1.5		W
Pdown	Power down mode		2		mW



DDR ELECTRICAL Characteristics and DC Operating Condition

Symbol	Parameters	Min	Typ	Max	Unit
RVDD(DDR333)	DDR I/O supply voltage for DDR266 or DDR333	2.3	2.5	2.7	V
RVDD(DDR400)	DDR I/O supply voltage for DDR400	2.5	2.6	2.7	V
DVREF	DDR I/O reference voltage	0.49*RVDD	0.5*RVDD	0.51*RVDD	V
VTT	DDR I/O termination voltage	VREF-0.04	VREF	VREF+0.04	V
VIH	DDR input voltage high	VREF+0.15		RVDD+0.3	V
VIL	DDR input voltage low	-0.3		VREF-0.15	V

DDR AC Operating Condition

Symbol	Parameters	Min	Typ	Max	Unit
VIH	Input high voltage, DQ, DQS	DVREF+0.31			V
VIL	Input low voltage, DQ, DQS			DVREF-0.31	V
Vslew	Input minimum slew rate	1.0			V/ns
Vswing	Input maximum swing			1.5	V

Digital Power Amplifier R2S15102NP

10Wx2ch(SE)/20Wx1ch(BTL) Digital Audio Power Amplifier

1.Outline

R2S15102NP is a Digital Power Amplifier IC developed for TV.
R2S15102NP can realize maximum Power 10W × 2ch
(VD = 24V, THD = 10%, SE) at 8 Ω load.
It is possible to replace from the conventional analog amplifier
system to the digital amplifier system easily.

2.Feature

High Output Power(THD=10%)without external Heat Sink
(note) the thermal pad is soldered the thermal pad with
the printed-circuit board directly.

Recommended Power Condition

SE operation mode :10Wx2ch(VD=24V) at 8 Ω

BTL operation mode: 20Wx1ch(VD=18V) at 8 Ω

The RENESAS original circuits realize high power efficiency,
low noise and low distortion characteristics.

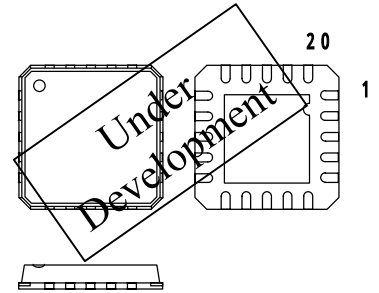
Pop sound Less

Built-in protection function

(Over Current, Over Temperature and Under Voltage)

Built-in Mute and Stand-by function

Fig. 1 Package



20pin QFN

Body : 6 x 6 mm

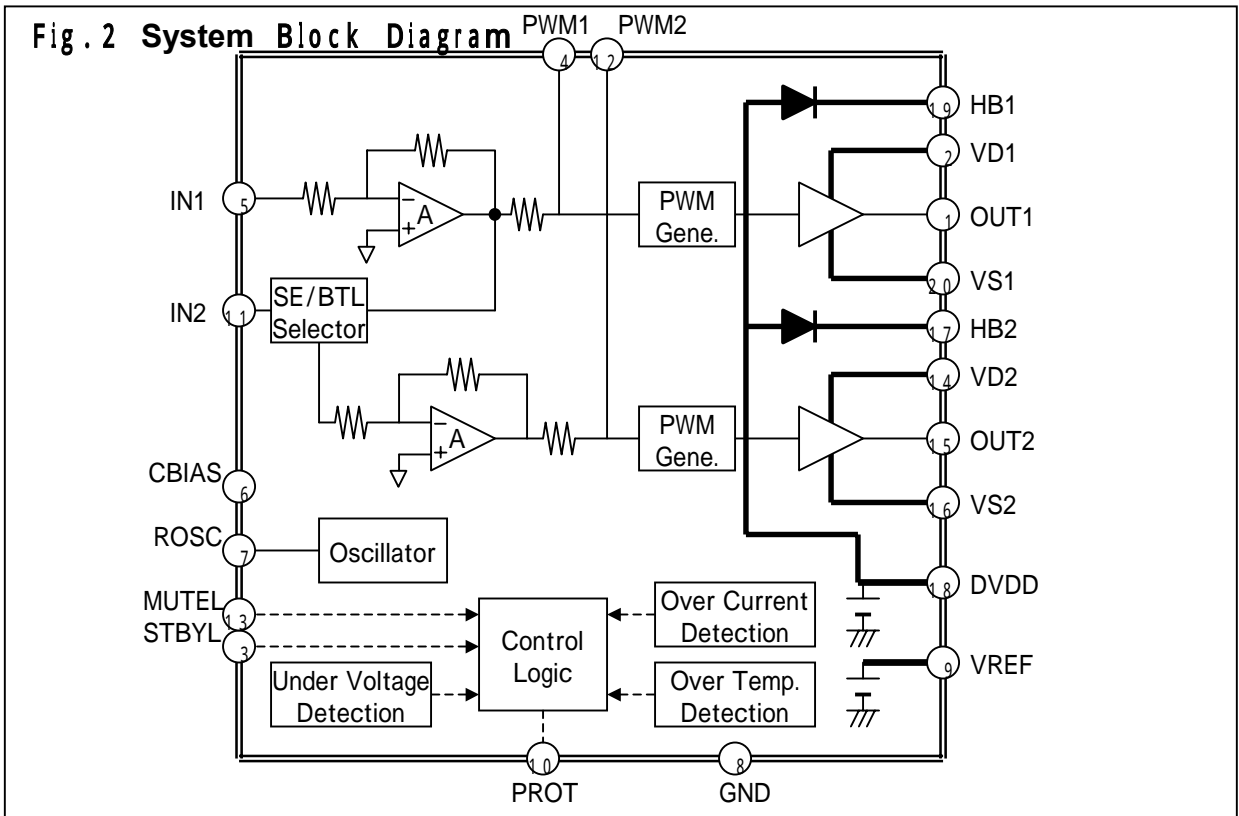
Lead pitch : 0.8 mm

3.Operating Condition

Recommended Power supply voltage : from 11V to 25V

Recommended Speaker Impedance : from 4 to 8Ω

4.Block Diagram



Digital Power Amplifier R2S15102NP

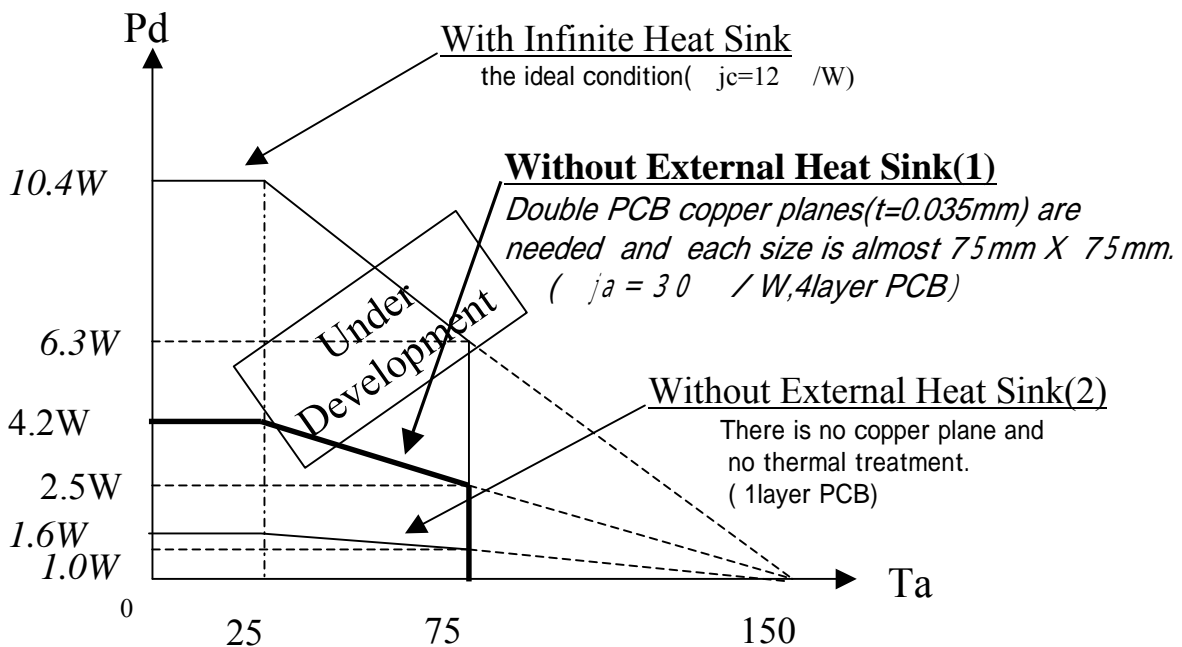
5 . Pin Configuration(Table.1)

No.	NAME	I/O	Description	
1	OUT1	O	Power Output pin #1	
2	VD1	-	Power supply pin for power output stage #2	
3	STBYL	I	Stand-by control pin. When this is “L”, circuit current is reduced. There is the pull-down resistor:50Kohm(typ.).	
4	PWM1	I	PWM input pin #1 (for phase compensation)	
5	IN1	I	Analog input #1. The gain is depended on the external resistance .	
6	CBIAS	I/O	A capacitor is connected so that it may not be influenced of power supply change(Ripple Filter).	
7	ROSC	I	Control pin for PWM carrier frequency	
8	GND	-	GND pin for analog block	
9	VREF	I/O	Capacitor connection pin for analog block reference voltage source	
10	PROT	O	Protection Timer pin. At protection mode,the output becomes “L”-level. (The timing capacitor is connected)	
11	IN2	I	SE operation	Analog input #2(as same as IN1)
		I	BTL operation	When this is connected to DVDD pin via the resistor, Reversed signal of OUT1 is output to OUT2.
12	PWM2	I	PWM input pin#2 (for phase compensation)	
13	MUTEL	I	Mute control pin. When this is “L”, it becomes mute status.	
14	VD2	-	Power supply pin for power output stage #2	
15	OUT2	O	Power Output pin #2	
16	VS2	-	Ground pin for power output stage #2	
17	HB2	I/O	Capacitor connection pin for bootstrap	
18	DVDD	O	Built-in power supply pin for internal digital block.	
19	HB1	I/O	Capacitor connection pin for bootstrap #1	
20	VS1	-	Ground pin for power output stage #1	

6 . Absolute Maximum Rating(Table.2)

Symbol	Parameter	Condition	Value	Unit
VD max	Maximum VD Voltage	VD1,VD2 pin voltage	27	V
HB max	Maximum HB Voltage	HB1, HB2 pin voltage	40	V
Pd	Power dispassion	Ta = 25°C :See Fig.3	4.2	W
ja	Thermal Resistance	See Fig.3	30	/W
Tj	Junction temperature	Maximum Temperature	150	
Ta	Operating ambient temperature	Temperature range	-20 ~ 75	
Tstg	Storage temperature	Temperature range	-40 ~ 150	

Fig.3 Thermal De-rating(on PCB: printed-circuit board):Size 75mm x 75mm

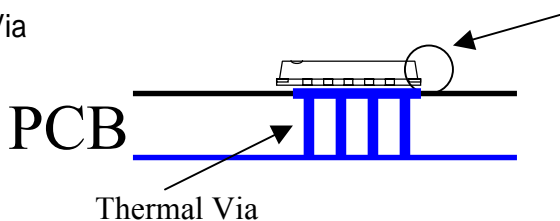


(NOTE)

PCB pattern design for high effective thermal conductivity

(1)The exposed die pad is **directly** soldered with the printed-circuit board pattern .

(2)Thermal Via



(caution)

There are side expositions of the die pad at corners of the package.

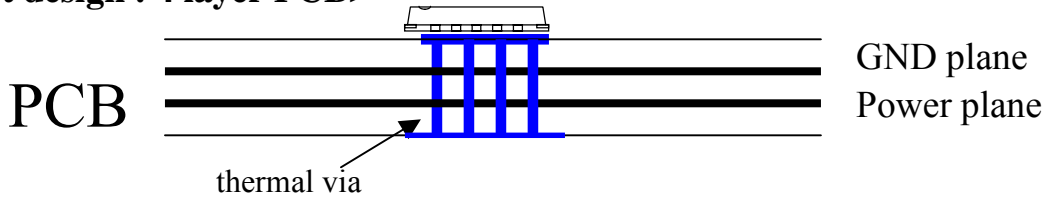
(The die pad is grounded.)

Consideration about the PCB design

The Power dissipation at 10Wx2ch(SE) or 20Wx1ch(BTL) is estimated almost 2W. It has enough margin, designing the PCB at $j_a=30$ /W.

(1)PCB basic design (copper plane)

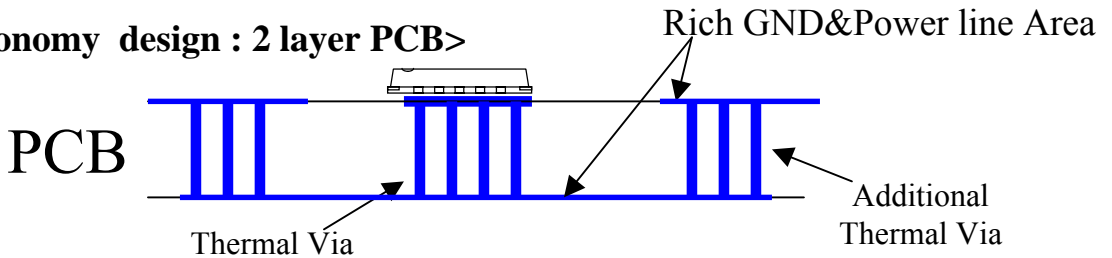
<the best design : 4 layer PCB>



<PCB size estimation >

10Wx2ch: 75mm x 75mm

<the economy design : 2 layer PCB>



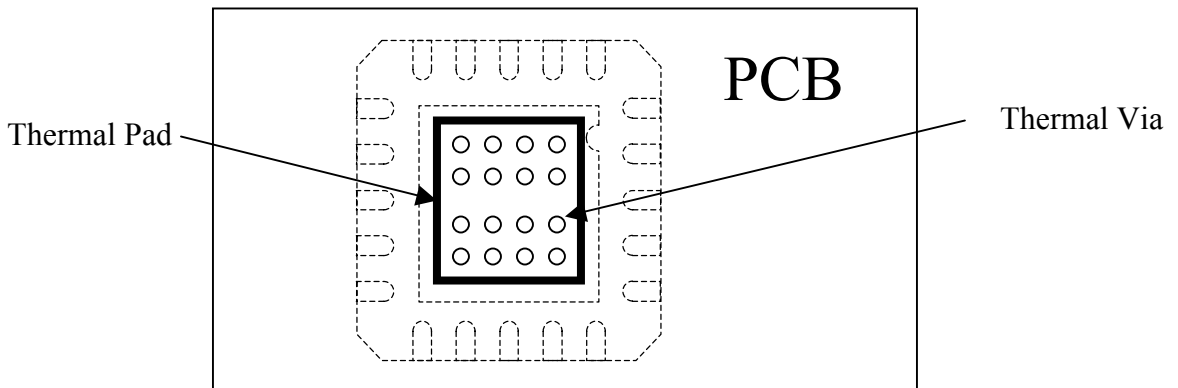
The GND&Power line total area size is also equal to the above GND&Power line total area size of the 4layer PCB.

<PCB size estimation >

10Wx2ch: (75+)mm x (75+) mm

(2)PCB Thermal Pad

The exposed die pad is **directly** soldered with the printed-circuit board pattern .



Digital Power Amplifier R2S15102NP

7 . Recommended Operating condition(Table.3)

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
VD	Supply Voltage	VD1,VD2 pin voltage	11	-	25	V
VH	Control voltage of high level	STBYL, MUTEL	2	-	5	V
VL	Control voltage of low level	STBYL, MUTEL	0	-	0.8	V
fosc	Carrier Frequency	R= 33k	300	400	600	kHz

- (note)
- STBYL: High level:normal operation Low level:Stand-by
 - MUTEL:High level:normal operation Low level:Mute
 - The carrier frequency can be changed by the resistance at Pin#.7 .

8 . Electronic Characteristics(Table.4)

(Unless otherwise noted, Ta=25°C, VD=24V, Carrier Frequency=400kHz, f=1kHz,SE operation)

Symbol	Parameter		Condition	MIN	TYP	MAX	Unit
IVD	Circuit Current		No Signal	TBD	28	TBD	mA
			MUTE	TBD	-	TBD	mA
			Stand-by	-	-	10	uA
VDPR	Detection Voltage		VD under-voltage	TBD	9.8	TBD	V
TPR	Protection Temperature		Thermal Shut-dawn	-	150	-	
TRL	Release Temperature		Thermal Shut-dawn	-	120	-	
IPR	Protection Current		Output over-current	-	6	-	A
Pomax	Maximum output power	at SE	THD=10%, VD=24V, RL=8	TBD	10	-	W/ch
		at BTL	THD=10%, VD=18V, RL=8	TBD	20	-	W
THD	Total Harmonic Distortion		Po=1W	-	0.1	TBD	%
No	Output Noise level		A-Weighted filter	-	(100)	TBD	uVrms
Eff	Power Efficiency	at SE	Po=10+10W	TBD	93	-	%
		at BTL	Po=20W	TBD	89	-	%
Mute	Mute Attenuation			TBD	80	-	dB
PSRR	Ripple Rejection Ratio		dVD=100mVrms,f=100 Hz	TBD	50	-	dB

9 . Application Examples

(note)

“R for GND” ‘s are for the evaluation only and not needed actually.

Fig.4 SE operation mode(10Wx2ch)

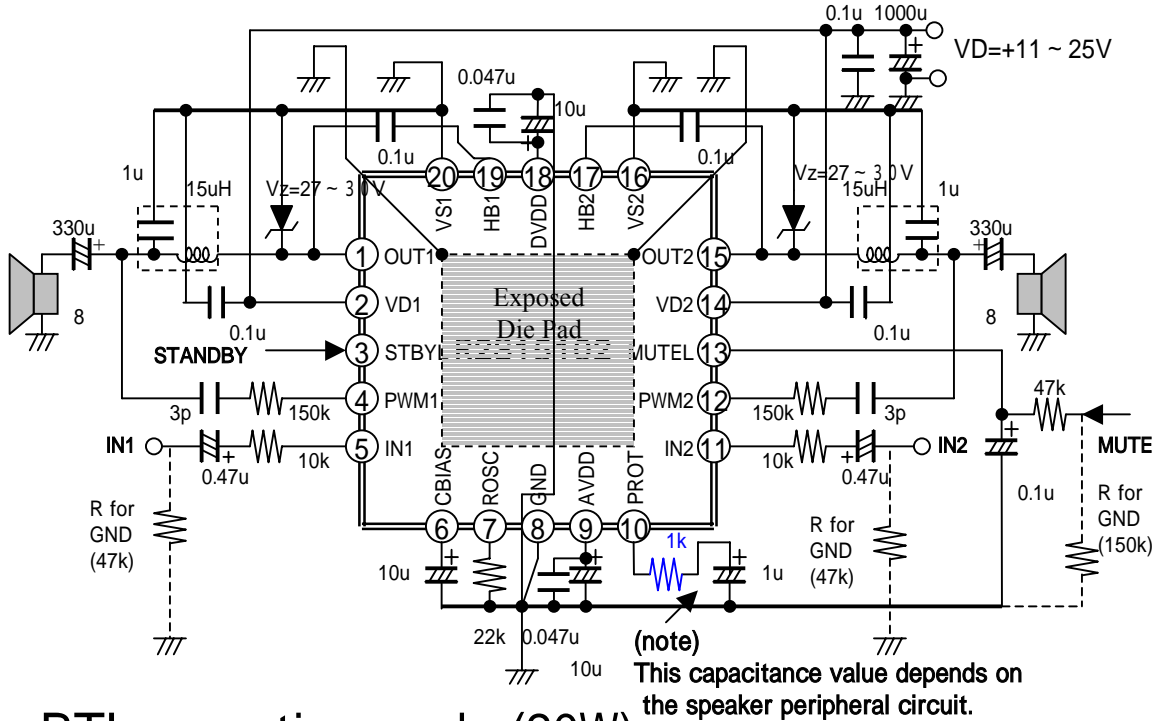
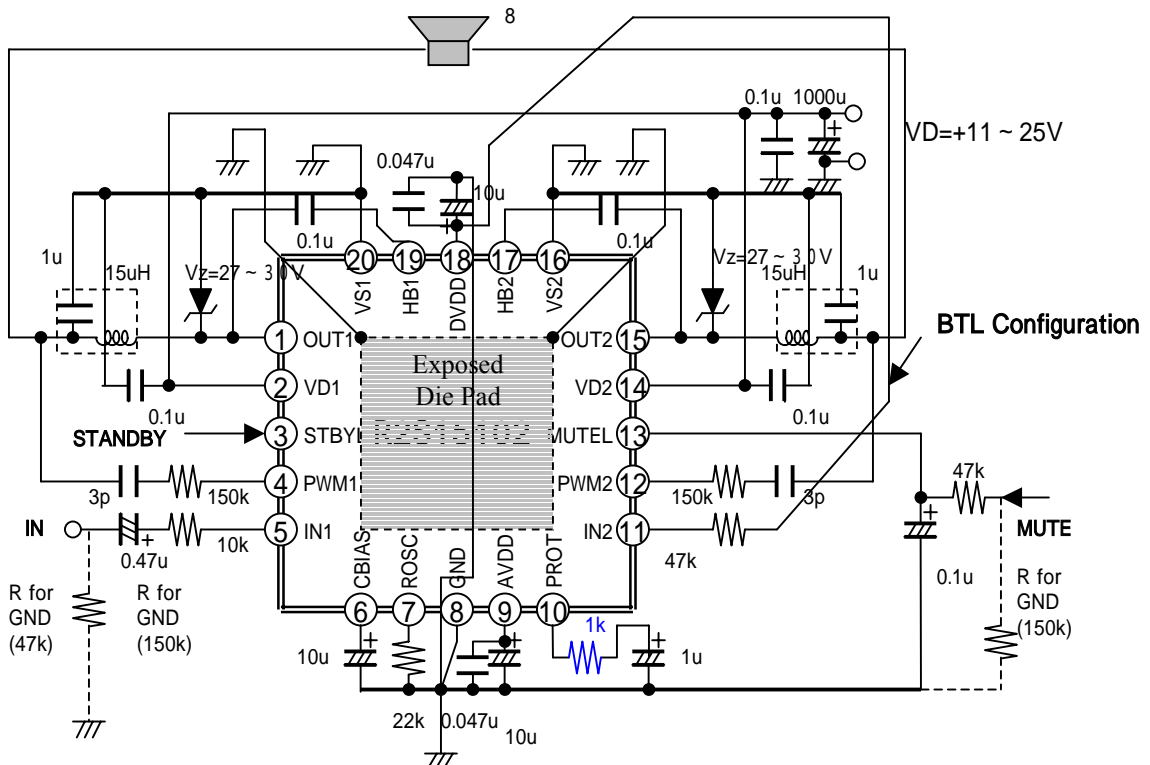


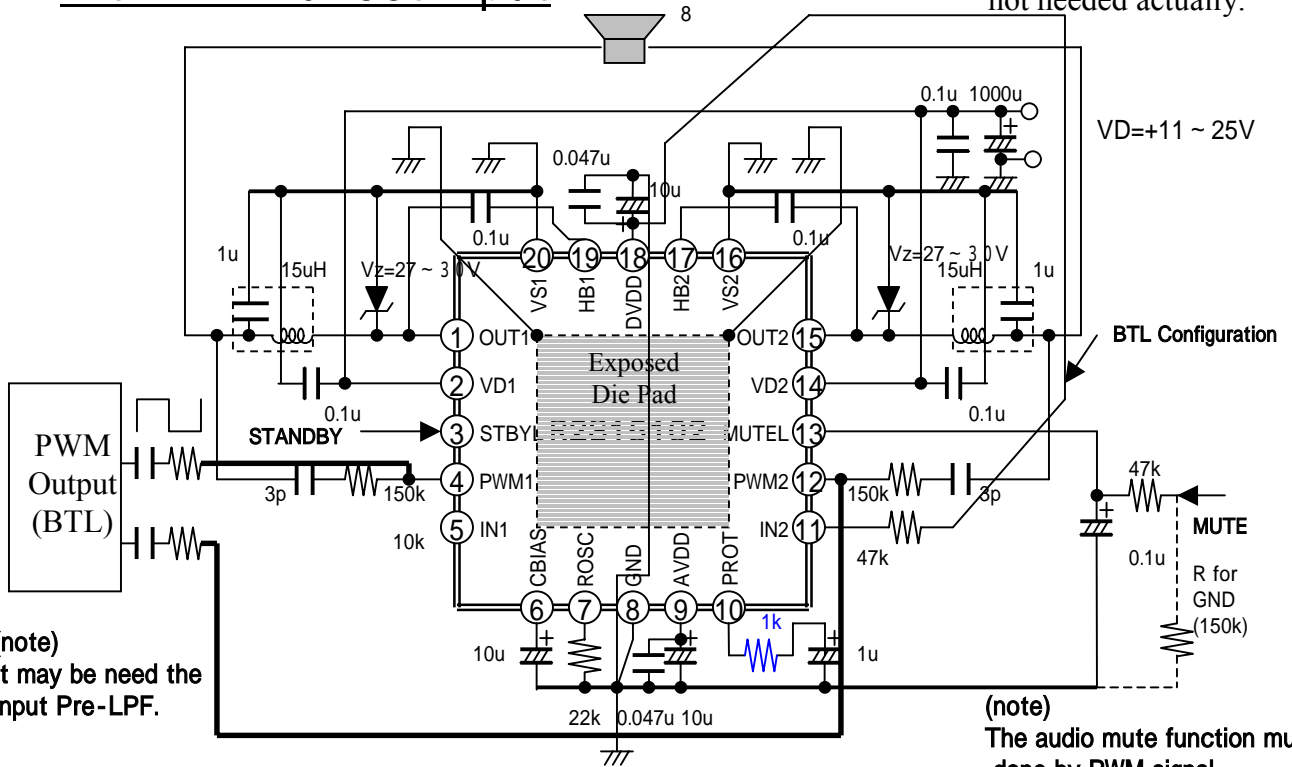
Fig.5 BTL operation mode (20W)



Digital Power Amplifier R2S15102NP

Fig.6 BTL operation mode(20W) with PWM direct input

(note)
“R for GND” ‘s are for the evaluation only and not needed actually.

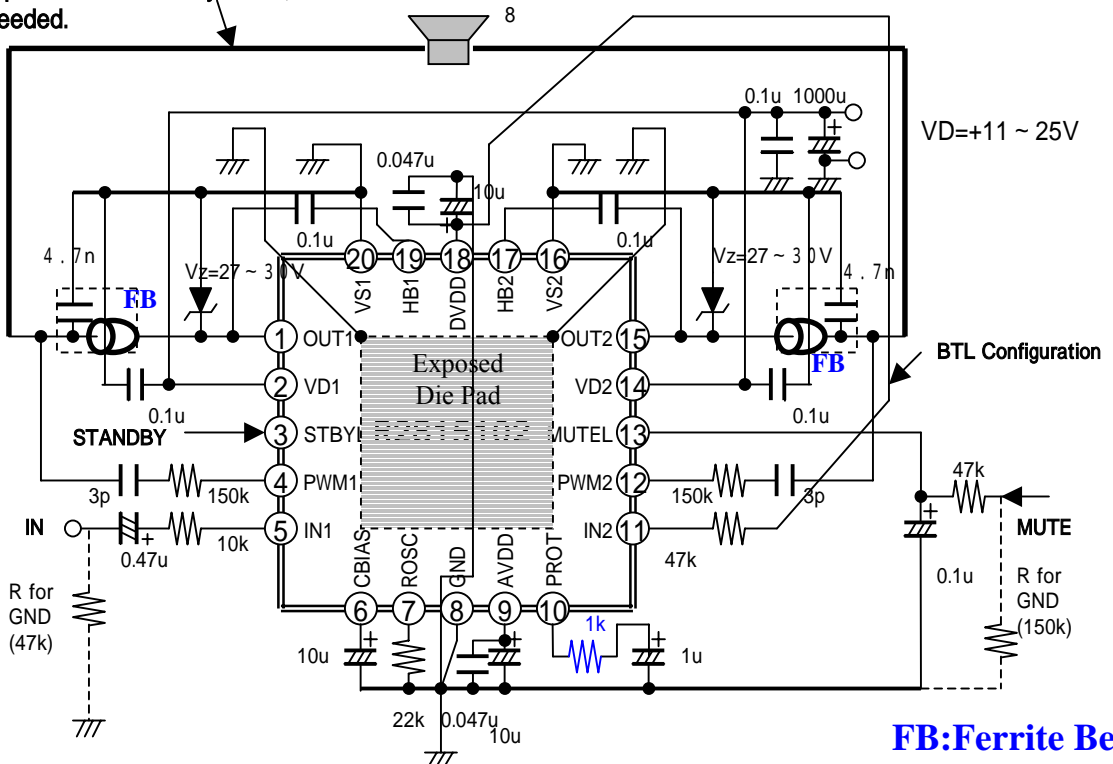


(note)
It may be need the input Pre-LPF.

(note)
The audio mute function must be done by PWM signal.

Fig.7 BTL operation mode without output LPF coil

If this speaker lines is very short, the LPF coil is not needed.



FB: Ferrite Beads

24-bit, 192kHz Stereo Codec with 5 Channel I/P Multiplexer

DESCRIPTION

The WM8776 is a high performance, stereo audio codec with five channel input selector. The WM8776 is ideal for surround sound processing applications for home hi-fi, DVD-RW and other audio visual equipment.

A stereo 24-bit multi-bit sigma delta ADC is used with a five stereo channel input mixer. Each ADC channel has programmable gain control with automatic level control. Digital audio output word lengths from 16-32 bits and sampling rates from 32kHz to 96kHz are supported.

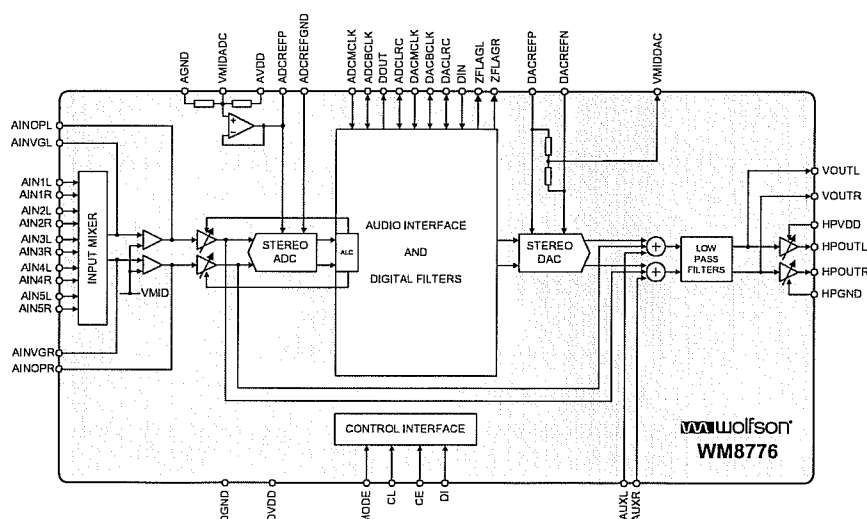
A stereo 24-bit multi-bit sigma delta DAC is used with digital audio input word lengths from 16-32 bits and sampling rates from 32kHz to 192kHz. The DAC has an input mixer allowing an external analogue signal to be mixed with the DAC signal. There are also Headphone and line outputs, with volume controls for the headphones.

The WM8776 supports fully independent sample rates for the ADC and DAC. The audio data interface supports I²S, left justified, right justified and DSP formats.

The device is controlled in software via a 2 or 3 wire serial interface, selected by the MODE pin, which provides access to all features including channel selection, volume controls, mutes, and de-emphasis facilities.

The device is available in a 48-pin TQFP package.

BLOCK DIAGRAM



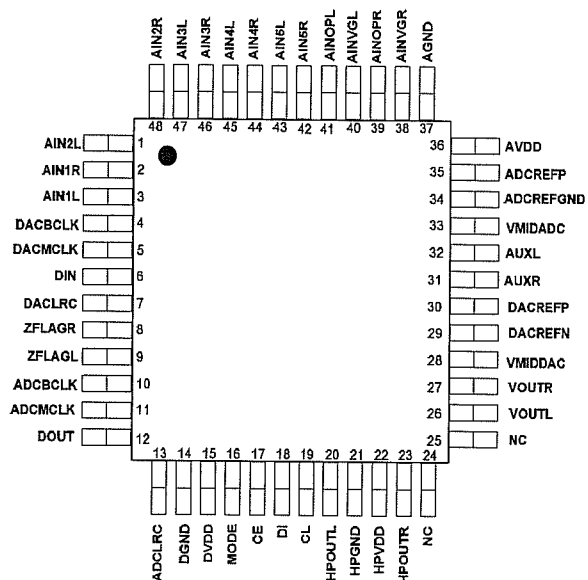
FEATURES

- Audio Performance
 - 108dB SNR ('A' weighted @ 48kHz) DAC
 - 102dB SNR ('A' weighted @ 48kHz) ADC
- DAC Sampling Frequency: 32kHz – 192kHz
- ADC Sampling Frequency: 32kHz – 96kHz
- Five stereo ADC inputs with analogue gain adjust from +24dB to –21dB in 0.5dB steps
- Programmable Limiter or Automatic Level Control (ALC)
- Stereo DAC with independent analogue and digital volume controls
- Stereo Headphone and Line Output
- 3-Wire SPI Compatible or 2-Wire Software Serial Control Interface
- Master or Slave Clocking Mode
- Programmable Audio Data Interface Modes
 - I²S, Left, Right Justified or DSP
 - 16/20/24/32 bit Word Lengths
- Analogue Bypass Path Feature
- Selectable AUX input to the volume controls
- 2.7V to 5.5V Analogue, 2.7V to 3.6V Digital supply Operation

APPLICATIONS

- Surround Sound AV Processors and Hi-Fi systems
- DVD-RW

PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8776EFT/V	-25 to +85°C	48-pin TQFP	MSL2	240°C
WM8776EFT/RV	-25 to +85°C	48-pin TQFP (tape and reel)	MSL2	240°C
WM8776SEFT/V	-25 to +85°C	48-pin TQFP (lead free)	MSL2	260°C
WM8776SEFT/RV	-25 to +85°C	48-pin TQFP (lead free, tape and reel)	MSL2	260°C

Note:

Reel quantity = 2,200

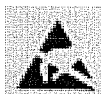
PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	AIN2L	Analogue Input	Channel 2 left input multiplexor virtual ground
2	AIN1R	Analogue Input	Channel 1 right input multiplexor virtual ground
3	AIN1L	Analogue Input	Channel 1 left input multiplexor virtual ground
4	DACBCLK	Digital input/output	DAC audio interface bit clock
5	DACMCLK	Digital input	Master DAC clock; 256, 384, 512 or 768fs (fs = word clock frequency)
6	DIN	Digital Input	DAC data input
7	DACLRC	Digital input/output	DAC left/right word clock
8	ZFLAGR	Open Drain output	DAC Right Zero Flag output (external pull-up resistor required)
9	ZFLAGL	Open Drain output	DAC Left Zero Flag output (external pull-up resistor required)
10	ADCBCLK	Digital input/output	ADC audio interface bit clock
11	ADCCLK	Digital input	ADC audio interface master clock
12	DOUT	Digital output	ADC data output
13	ADCLRC	Digital input/output	ADC left/right word clock
14	DGND	Supply	Digital negative supply
15	DVDD	Supply	Digital positive supply
16	MODE	Digital input	Control interface mode select (5V tolerant)
17	CE	Digital input	Serial interface Latch signal (5V tolerant)
18	DI	Digital input	Serial interface data (5V tolerant)
19	CL	Digital input	Serial interface clock (5V tolerant)
20	HPOUTL	Analogue Output	Headphone left channel output
21	HPGND	Supply	Headphone negative supply
22	HPVDD	Supply	Headphone positive supply
23	HPOUTR	Analogue Output	Headphone right channel output
24	NC	Not bonded	
25	NC	Not bonded	
26	VOUTL	Analogue output	DAC channel left output
27	VOUTR	Analogue output	DAC channel right output
28	VMIDDAC	Analogue output	DAC midrail decoupling pin ; 10uF external decoupling
29	DACREFN	Analogue input	DAC negative reference input
30	DACREFP	Analogue input	DAC positive reference input
31	AUXR	Analogue input	DAC mixer right channel input
32	AUXL	Analogue input	DAC mixer left channel input
33	VMIDADC	Analogue Output	ADC midrail divider decoupling pin; 10uF external decoupling
34	ADCREFGND	Supply	ADC negative supply and substrate connection
35	ADCREFP	Analogue Output	ADC positive reference decoupling pin; 10uF external decoupling
36	AVDD	Supply	Analogue positive supply
37	AGND	Supply	Analogue negative supply and substrate connection
38	AINVGR	Analogue Input	Right channel multiplexor virtual ground
39	AINOPR	Analogue Output	Right channel multiplexor output
40	AINVGL	Analogue Input	Left channel multiplexor virtual ground
41	AINOPL	Analogue Output	Left channel multiplexor output
42	AIN5R	Analogue Input	Channel 5 right input multiplexor virtual ground
43	AIN5L	Analogue Input	Channel 5 left input multiplexor virtual ground
44	AIN4R	Analogue Input	Channel 4 right input multiplexor virtual ground
45	AIN4L	Analogue Input	Channel 4 left input multiplexor virtual ground
46	AIN3R	Analogue Input	Channel 3 right input multiplexor virtual ground
47	AIN3L	Analogue Input	Channel 3 left input multiplexor virtual ground
48	AIN2R	Analogue Input	Channel 2 right input multiplexor virtual ground

Note : Digital input pins have Schmitt trigger input buffers and pins 16, 17, 18 and 19 are 5V tolerant.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+3.63V
Analogue supply voltage	-0.3V	+7V
Voltage range digital inputs (DI, CL, CE and MODE)	DGND -0.3V	+7V
Voltage range digital inputs (MCLK, DIN, ADCLRC, DACLRC, ADCBCLK and DACBCLK)	DGND -0.3V	DVDD + 0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Master Clock Frequency		37MHz
Operating temperature range, T _A	-25°C	+85°C
Storage temperature	-65°C	+150°C

Notes:

- Analogue and digital grounds must always be within 0.3V of each other.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		2.7		3.6	V
Analogue supply range	AVDD, HPVDD, DACREFP		2.7		5.5	V
Ground	AGND, DGND, DACREFN, ADCREFGND			0		V
Difference DGND to AGND			-0.3	0	+0.3	V

Note: digital supply DVDD must never be more than 0.3V greater than AVDD.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (TTL Levels)						
Input LOW level	V _{IL}				0.8	V
Input HIGH level	V _{IH}		2.0			V
Output LOW	V _{OL}	I _{OL} =1mA			0.1 x DVDD	V
Output HIGH	V _{OH}	I _{OH} =1mA	0.9 x DVDD			V
Analogue Reference Levels						
Reference voltage	V _{V_{MID}}			AVDD/2		V
Potential divider resistance	R _{V_{MID}}			50k		Ω
DAC Performance (Load = 10k Ω, 50pF)						
0dBfs Full scale output voltage				1.0 x AVDD/5		V _{rms}
SNR (Note 1,2)		A-weighted, @ fs = 48kHz		108		dB
SNR (Note 1,2)		A-weighted @ fs = 96kHz		108		dB
Dynamic Range (Note 2)	DNR	A-weighted, -60dB full scale input		108		dB
Total Harmonic Distortion (THD)		1kHz, 0dBfs		-97	-90	dB
DAC channel separation				100		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Headphone Buffer						
Maximum Output voltage				0.9		V _{rms}
Max Output Power (Note 4)	P _o	R _L = 32 Ω		25		mW
		R _L = 16 Ω		50		mW
SNR (Note 1,2)		A-weighted	85	92		dB
Headphone analogue Volume Gain Step Size			0.5	1	1.5	dB
Headphone analogue Volume Gain Range		1kHz Input	-73		+6	dB
Headphone analogue Volume Mute Attenuation		1kHz Input, 0dB gain		100		dB
Total Harmonic Distortion +Noise	THD+N	1kHz, R _L = 32Ω @ P _o = 10mW rms		-80 0.01	-60 0.1	dB %
		1kHz, R _L = 32Ω @ P _o = 20mW rms		-77 0.014	-40 1.0	dB %
Power Supply Rejection Ratio	PSRR	20Hz to 20kHz, without supply decoupling		-40		dB
ADC Performance						
Input Signal Level (0dB)				1.0 x AVDD/5		V _{rms}
SNR (Note 1,2)		A-weighted, 0dB gain @ fs = 48kHz		102		dB
SNR (Note 1,2)		A-weighted, 0dB gain @ fs = 96kHz 64 x OSR		100		dB
Dynamic Range (note 2)		A-weighted, -60dB full scale input		102		dB
Total Harmonic Distortion (THD)		1kHz, 0dBfs		-90	-80	DB

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, f_s = 48kHz, MCLK = 256fs unless otherwise stated.

		1kHz, -3dBFS		-95	-85	dB
ADC Channel Separation		1kHz Input		90		dB
Programmable Gain Step Size			0.25	0.5	0.75	dB
Programmable Gain Range (Analogue)		1kHz Input	-21		+24	dB
Programmable Gain Range (Digital)		1kHz Input	-103		-21.5	dB
Mute Attenuation (Note 6)		1kHz Input, 0dB gain		76		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Analogue input (AIN) to Analogue output (VOUT) (Load=10k Ω, 50pF, gain = 0dB) Bypass Mode						
0dB Full scale output voltage				1.0 x AVDD/5		V _{rms}
SNR (Note 1)			90	100		dB
THD		1kHz, 0dB		-90		dB
		1kHz, -3dB		-95		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Mute Attenuation		1kHz, 0dB		100		dB
Supply Current						
Analogue supply current		AVDD = 5V		48		mA
Digital supply current		DVDD = 3.3V		8		mA

Notes:

- Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted.
- All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
- VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).
- Harmonic distortion on the headphone output decreases with output power.
- All performance measurement done using certain timings conditions (Please refer to section 'Digital Audio Interface').
- A better MUTE Attenuation can be achieved if the ADC gain is set to minimum.

TERMINOLOGY

- Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
- Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB = -32dB, DR = 92dB).
- THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
- Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside audio band).
- Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
- Pass-Band Ripple - Any variation of the frequency response in the pass-band region.

TFT LCD Preliminary Specification

MODEL NO.: V370H1 - L0A
(For L02/L03 Mechanical Compatibility)

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 1.0	Dec,12,'05	All	All	Preliminary Specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V370H1-L0A is a 37" thin-film-transistor liquid-crystal (TFT-LCD) module with 20-CCFL Backlight unit and 2ch-LVDS interface. This module supports 1920 x 1080 HDTV format and can display true 16.7M colors (8-bit/color). The inverter module for backlight is built-in.

1.2 FEATURES

- Ultra wide viewing angle – Super MVA technology
- High brightness (500 nits)
- High contrast ratio > 1100:1
- Fast response time < 8 ms
- High color saturation (NTSC 75%)
- HD (1920 x 1080 pixels) resolution
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface

1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- MFM Application.

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	820.8 (H) x 461.7 (V) (37.07" diagonal)	mm	(1)
Bezel Opening Area	828.8 (H) x 470.9 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.1425 (H) x 0.4275 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-Glare coating Hard coating (3H)	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec of the surface treatment is temporarily for this phase. CMO reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note	
Module Size	Horizontal(H)	884.1	884.8	885.5	mm	
	Vertical(V)	525.3	525.9	526.5	mm	
	Depth(D)	43.34	44.34	45.34	mm	To PCB cover
	Depth(D)	50.34	51.84	53.34	mm	To inverter cover
Weight	9800	10000	10200	g		

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T_{OP}	0	50	°C	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	50	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

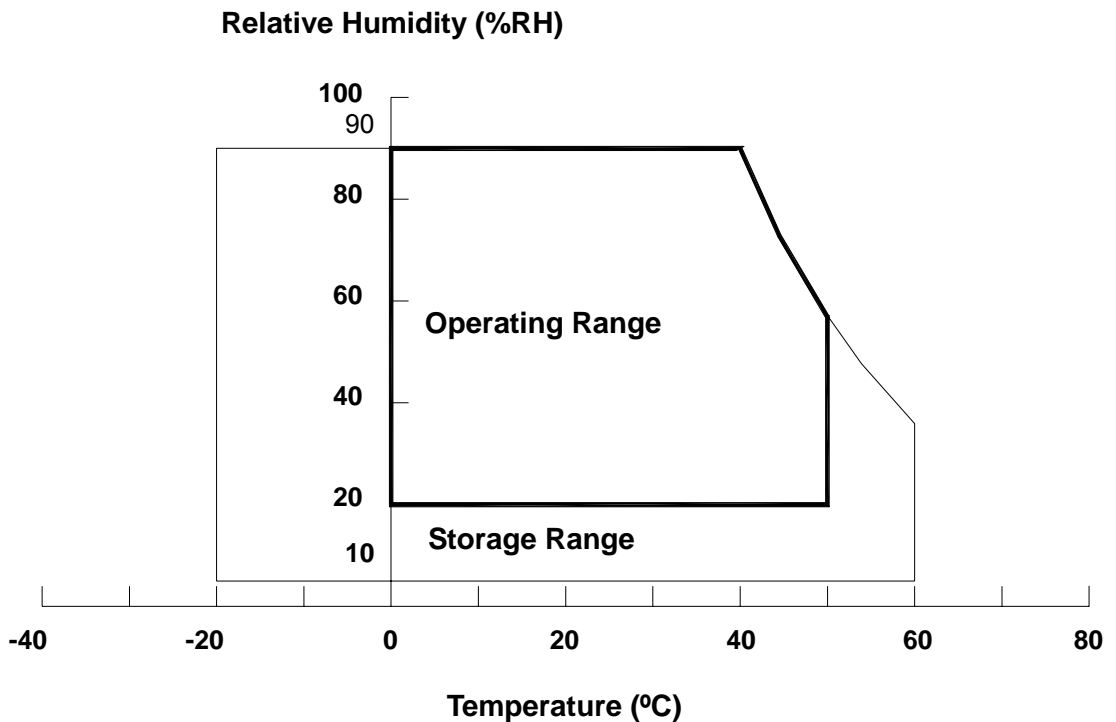
- (a) 90 %RH Max. ($T_a \leq 40\text{ °C}$).
- (b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40\text{ °C}$).
- (c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 60 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in your product design to prevent the surface temperature of display area from being over 60 °C. The range of operating temperature may degrade in case of improper thermal management in your product design.

Note (3) 11 ms, half sine wave, 1 time for $\pm X$, $\pm Y$, $\pm Z$.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture. The module would not be twisted or bent by the fixture.



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	20	V	(1)
Logic Input Voltage	V_{IN}	-0.3	3.6	V	

Note: (1) Permanent damage to the device may occur if maximum values are exceeded. Functional operation should be restricted to the conditions described under normal operating conditions.

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_W	-	5000	V_{RMS}	
Power Supply Voltage	V_{BL}	0	30	V	(1)
Control Signal Level	-	-0.3	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals includes On/Off Control, Internal PWM Control

3. ELECTRICAL CHARACTERISTICS

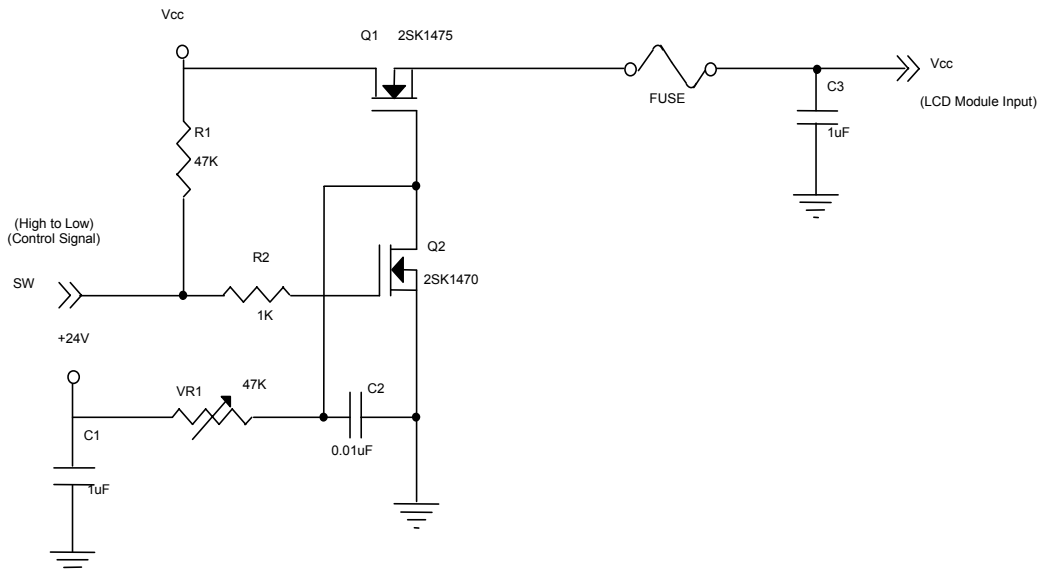
3.1 TFT LCD MODULE

Ta = 25 ± 2 °C

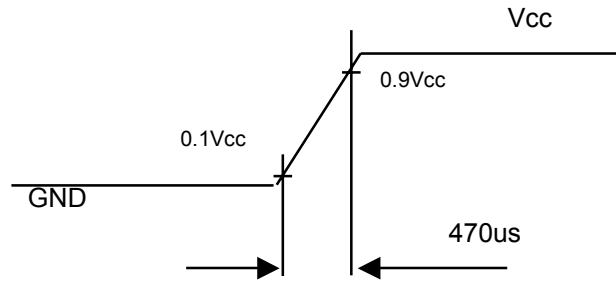
Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Supply Voltage	V _{CC}	10.8 16.2	12 18	13.2 19.8	V	(1)
Power Supply Ripple Voltage	V _{RP}	-	-	200	mV	
Rush Current	I _{RUSH}	-	-	4.5	A	(2)
Power Supply Current (at V _{CC} = 18)	White	-	1.0	-	A	(3)
	Black	-	0.5	-	A	
	Vertical Stripe	-	TBD	-	A	
Power Supply Current (at V _{CC} = 12)	White	-	1.5	-	A	
	Black	-	0.7	-	A	
	Vertical Stripe	-	TBD	-	A	
LVDS Interface	Differential Input High Threshold Voltage	V _{LVTH}	-	-	+100	mV
	Differential Input Low Threshold Voltage	V _{LVTL}	-100	-	-	mV
	Common Input Voltage	V _{LVC}	1.125	1.25	1.375	V
	Terminating Resistor	R _T	-	100	-	ohm
CMOS interface	Input High Threshold Voltage	V _{IH}	2.7	-	3.3	V
	Input Low Threshold Voltage	V _{IL}	0	-	0.7	V

Note: (1) The module should be always operated within either the 12V or 18V range.

(2) Measurement condition:

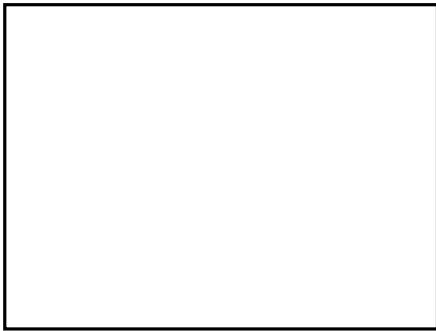


Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at $V_{cc} = 1.8 / 1.2V$, $T_a = 25 \pm 2 \text{ }^\circ\text{C}$, $f_v = 60 \text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern



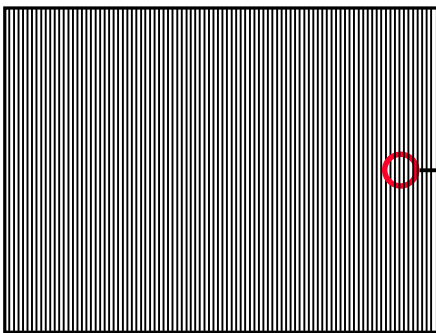
Active Area

b. Black Pattern

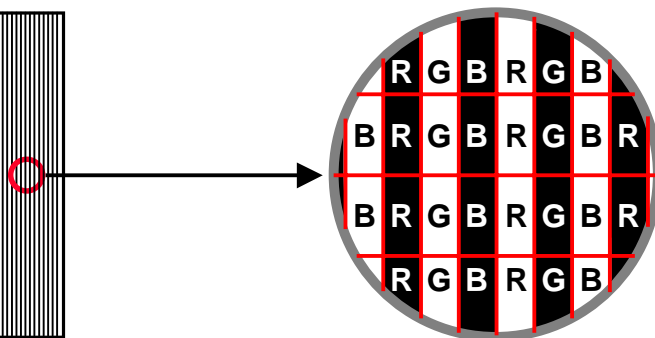


Active Area

c. Vertical Stripe Pattern



Active Area



3.2 BACKLIGHT UNIT

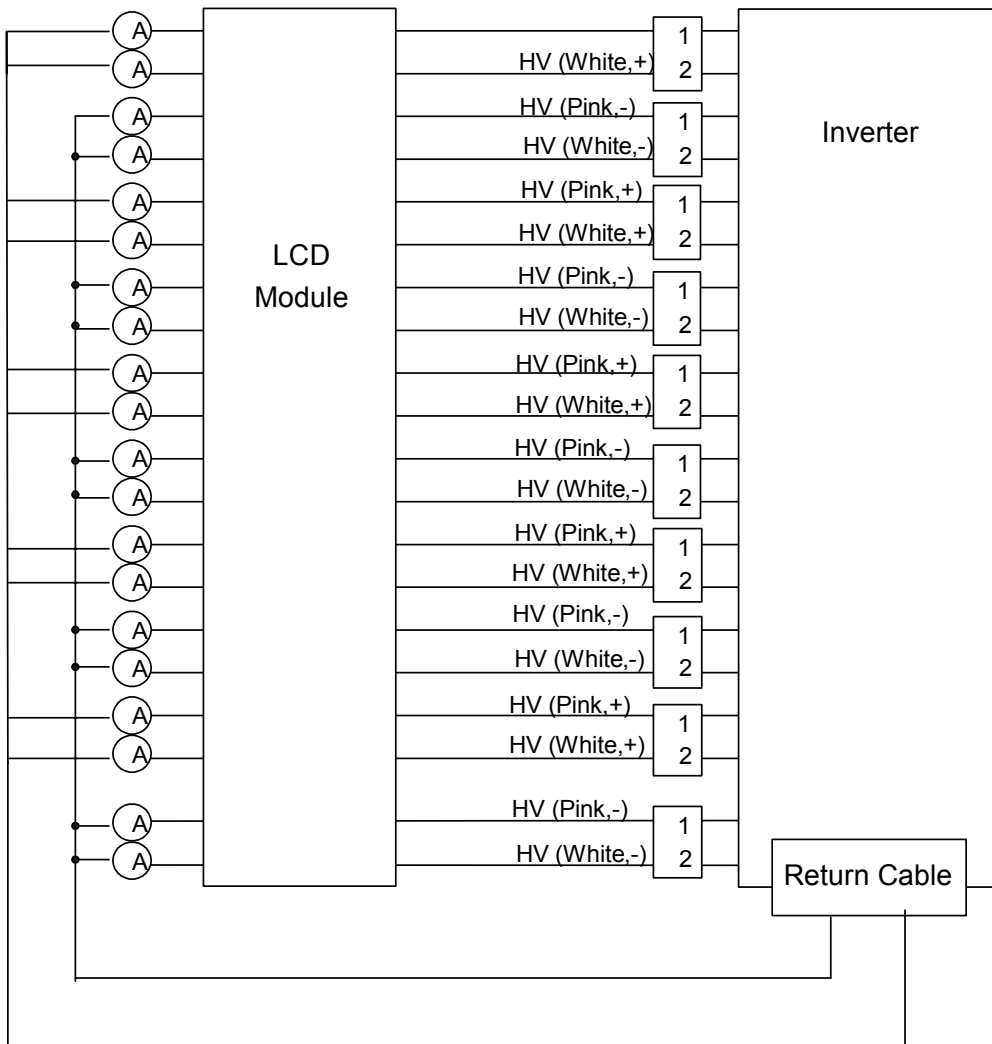
3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS (Ta=25±2)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Voltage	V _W	-	(1320)	-	V _{RMS}	I _L = 5.2mA
Lamp Current	I _L	4.7	5.2	5.7	mA _{RMS}	(1)
Lamp Starting Voltage	V _S	-	-	(2780)	V _{RMS}	(2), Ta = 0 °C
		-	-	(2440)	V _{RMS}	(2), Ta = 25 °C
Operating Frequency	F _o	40	-	70	KHz	(3)
Lamp Life Time	L _{BL}	50,000	60,000	-	Hrs	(4)

3.2.2 INVERTER CHARACTERISTICS (Ta =25±2)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power consumption	P _{BL}	-	151.2	-	W	(5), I _L = 5.2mA
Power Supply Voltage	V _{BL}	22.8	24	25.2	V _{DC}	
Power Supply Current	I _{BL}	-	6.3	-	A	Non Dimming
Input Ripple Noise	-	-	-	500	mVp-p	V _{BL} =22.8V
Backlight Turn on Voltage	V _{BS}	2780	-	-	V _{RMS}	Ta = 0 °C
	-	2440	-	-	V _{RMS}	Ta = 25 °C
Oscillating Frequency	F _W	49	50	51	kHz	
Dimming frequency	F _B	150	160	170	Hz	
Minimum Duty Ratio	D _{MIN}	-	20	-	%	

Note (1) Lamp current is measured by utilizing high frequency current meters as shown below:



Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second under starting up duration. Otherwise the lamp could not be lighted on completely.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point.) as the time in which it continues to operate under the condition

$$T_a = 25 \pm 2 \quad \text{and} \quad I_L = 4.7 \sim 5.7 \text{mA}_{\text{RMS}}$$

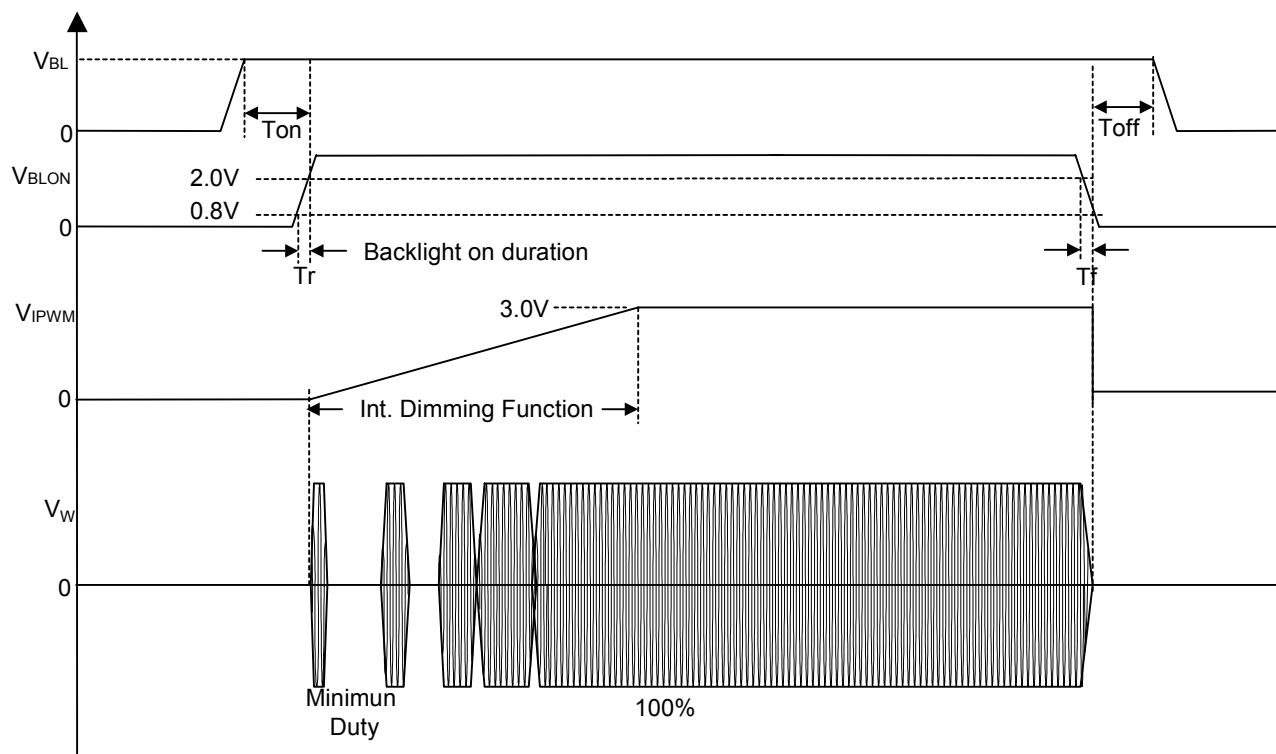
Note (5) The power supply capacity should be higher than the total inverter power consumption P_{BL} . Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of the power supply should be considered for the changing loading when inverter dimming.

3.2.3 INVERTER INTERFACE CHARACTERISTICS

Parameter	Symbol	Test Condition	Value			Unit	Note	
			Min.	Typ.	Max.			
On/Off Control Voltage	ON	V_{BLON}	-	2.0	-	5.0	V	
	OFF		-	0	-	0.8	V	
Internal PWM Control Voltage	MAX	V_{IPWM}	-	-	-	3.0	V	maximum duty ratio
	MIN		-	-	0	-	V	minimum duty ratio
Control Signal Rising Time	T_r	-	-	-	100	ms		
Control Signal Falling Time	T_f	-	-	-	100	ms		
Input impedance	R_{IN}	-	1	-	-	M		
BLON Delay Time1	T_{on1}	-	1	-	-	ms		
BLON Off Time1	T_{off1}	-	1	-	-	ms		

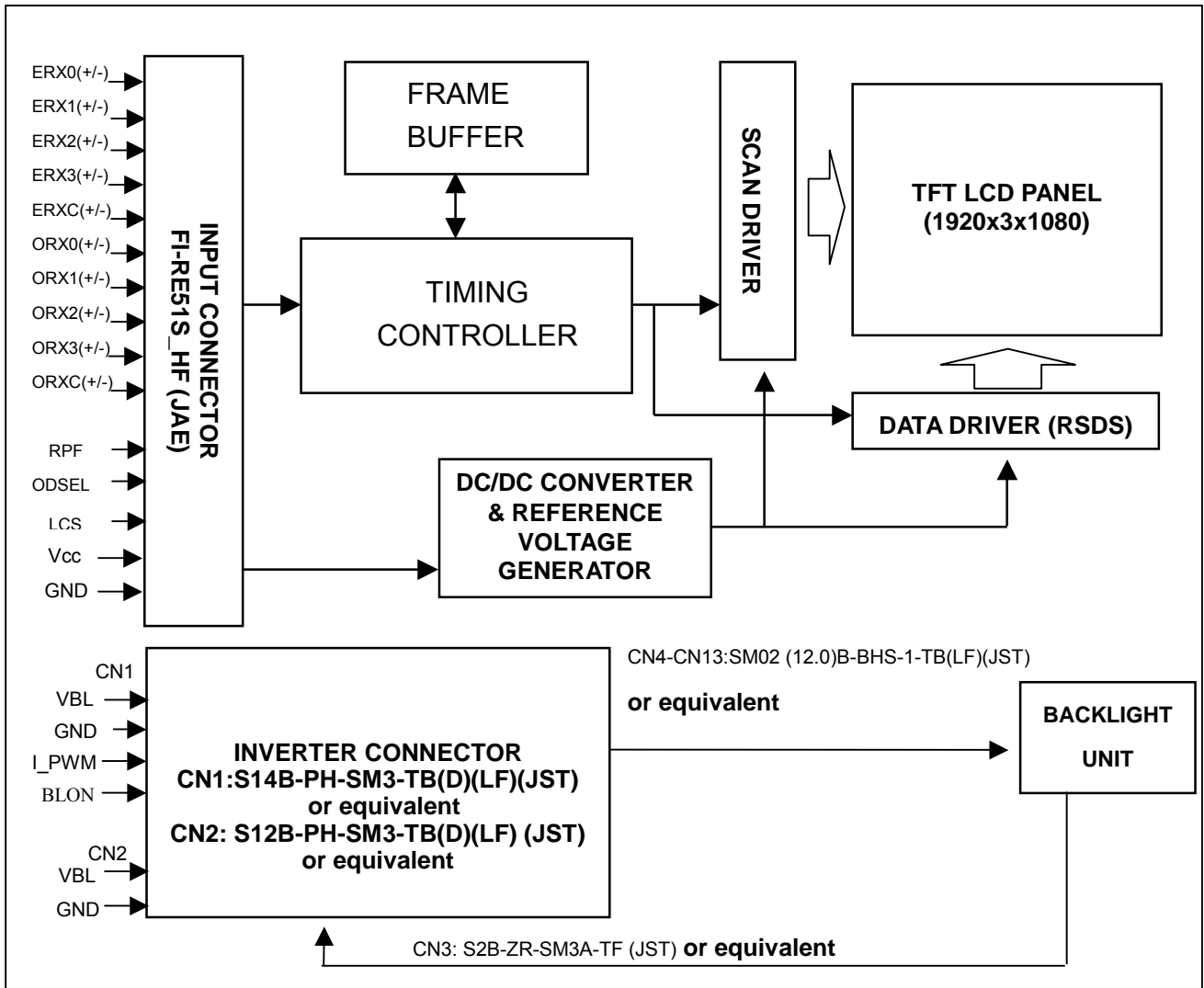
Note (1) The power sequence and control signal timing are shown in the following figure.

Note (2) The power sequence and control signal timing must follow the figure below. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.



4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



5. V370H1-L03 LCD INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE LVDS input

CNF1 Connector Pin Assignment :FI-RE51S-HF (JAE)

Pin	Name	Description	Note
1	GND	Ground	
2	N.C.	No Connection	(1)
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	
7	NC	No Connection	
8	RPF	Display Rotation	(2)
9	ODSEL	Overdrive Lookup Table Selection	(3)
10	LCS	Low Color Shift	(4)
11	GND	Ground	
12	ORX0-	Odd pixel, Negative LVDS differential data input. Channel 0	
13	ORX0+	Odd pixel, Positive LVDS differential data input. Channel 0	
14	ORX1-	Odd pixel, Negative LVDS differential data input. Channel 1	
15	ORX1+	Odd pixel, Positive LVDS differential data input. Channel 1	
16	ORX2-	Odd pixel, Negative LVDS differential data input. Channel 2	
17	ORX2+	Odd pixel, Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	OCLK-	Odd pixel, Negative LVDS differential clock input.	
20	OCLK+	Odd pixel, Positive LVDS differential clock input.	
21	GND	Ground	
22	ORX3-	Odd pixel, Negative LVDS differential data input. Channel 3	
23	ORX3+	Odd pixel, Positive LVDS differential data input. Channel 3	
24	N.C.	No Connection	(1)
25	N.C.	No Connection	
26	N.C.	No Connection	
27	N.C.	No Connection	
28	ERX0-	Even pixel, Negative LVDS differential data input. Channel 0	
29	ERX0+	Even pixel, Positive LVDS differential data input. Channel 0	
30	ERX1-	Even pixel, Negative LVDS differential data input. Channel 1	
31	ERX1+	Even pixel, Positive LVDS differential data input. Channel 1	
32	ERX2-	Even pixel, Negative LVDS differential data input. Channel 2	

33	ERX2+	Even pixel, Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	ECLK-	Even pixel, Negative LVDS differential clock input.	
36	ECLK+	Even pixel, Positive LVDS differential clock input.	
37	GND	Ground	
38	ERX3-	Even pixel, Negative LVDS differential data input. Channel 3	
39	ERX3+	Even pixel, Positive LVDS differential data input. Channel 3	
40	N.C.	No Connection	(1)
41	N.C.	No Connection	
42	N.C.	No Connection	
43	N.C.	No Connection	
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	GND	Ground	
48	VCC	Power input (+12V or +18.0V)	
49	VCC	Power input (+12V or +18.0V)	
50	VCC	Power input (+12V or +18.0V)	
51	VCC	Power input (+12V or +18.0V)	

Note (1) N.C.: Reserved for internal use. Please leave it open.

Note (2) Low : normal display (default), High : display with 180 degree rotation

Note (3) Overdrive lookup table selection. The overdrive lookup table should be selected in accordance to the frame rate to optimize image quality.

ODSEL	Note
L	Lookup table was optimized for 60 Hz frame rate.
H	Lookup table was optimized for 50 Hz frame rate.

Note (4) Low : normal display (default), High : Low Color Shift function enable.

5.3 BACKLIGHT UNIT

The pin configuration for the housing and the leader wire is shown in the table below.

CN4-CN13 (Housing): BHR-04VS-1

Pin	Name	Description	Wire Color
1	HV	High Voltage	Pink
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model BHR-04VS-1, manufactured by JST.

The mating header on inverter part number is SM02(12.0)B-BHS-1-TB.

5.4 INVERTER UNIT

CN1 (Header): S14B-PH-SM3-TB (D)(LF)(JST) or equivalent.

Pin No.	Symbol	Description
1	VBL	+24V _{DC} power input
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	SEL	Internal/external PWM selection High : external dimming Low : internal dimming
12	E_PWM	External PWM control signal E_PWM should be connected to ground when internal PWM was selected (SEL = low).
13	I_PWM	Internal PWM Control Signal
14	BLON	Backlight on/off control

CN2 (Header): S12B-PH-SM3-TB (D)(LF)(JST) or equivalent.

Pin No.	Symbol	Description
1	VBL	+24V _{DC} power input
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	NC	NC
12	NC	NC

CN3 (Header): S2B-ZR-SM3A-TF (JST) or equivalent

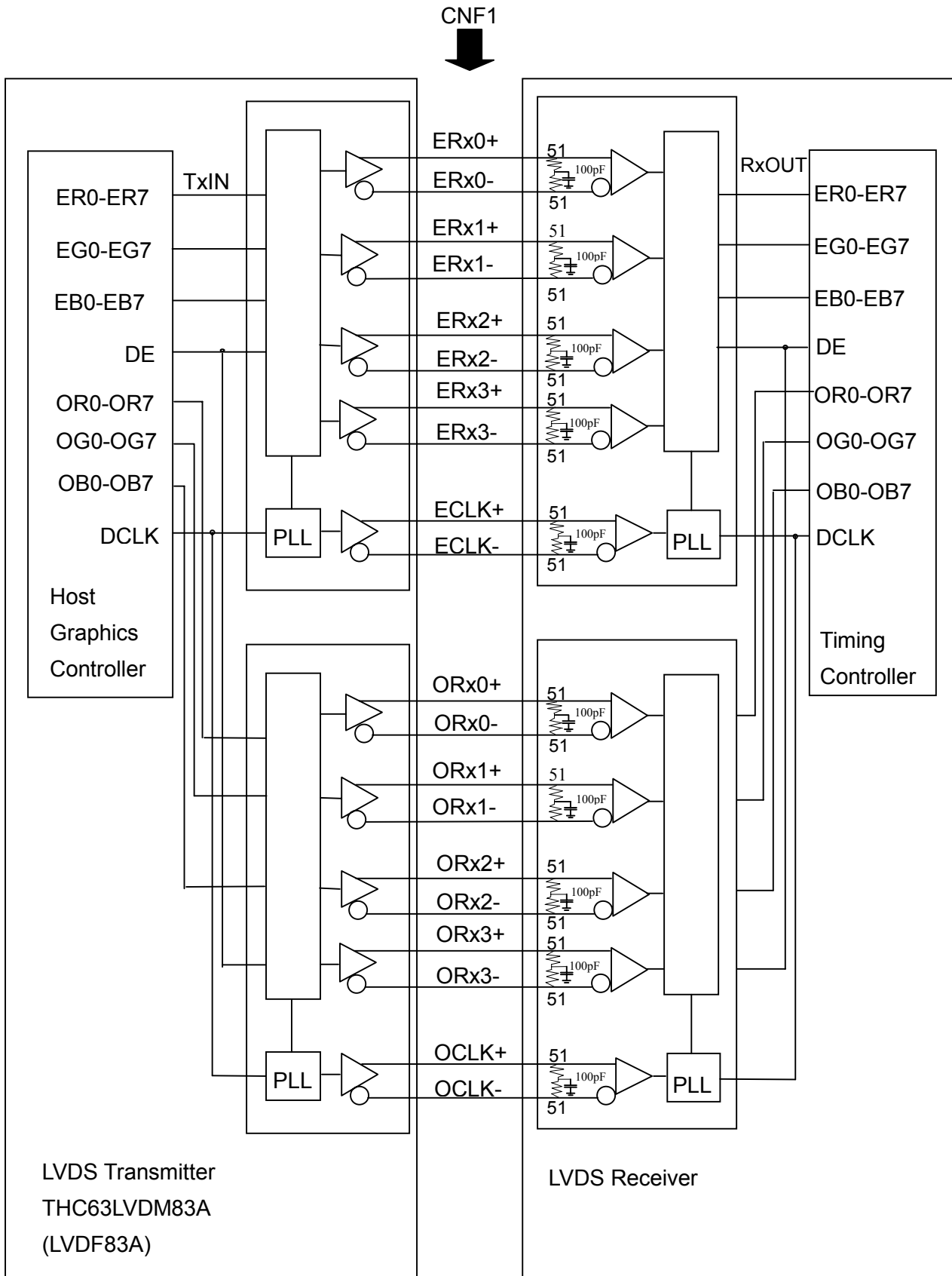
Pin No.	Symbol	Description
1	CCFL Cold	CFL Low voltage
2	CCFL Cold	CFL Low voltage

CN4-CN13 (Header): SM02(12.0)B-BHS-1-TB (LF)(JST) or equivalent

Pin No.	Symbol	Description
1	CCFL HOT	CCFL high voltage
2	CCFL HOT	CCFL high voltage

Note (1) Floating of any control signal is not allowed.

5.5 BLOCK DIAGRAM OF INTERFACE



ER0~ER7 : Even pixel R data
EG0~EG7 : Even pixel G data
EB0~EB7 : Even pixel B data
OR0~OR7 : Odd pixel R data
OG0~OG7 : Odd pixel G data
OB0~OB7 : Odd pixel B data
DE : Data enable signal
DCLK : Data clock signal

- Notes:
- (1) The system must have the transmitter to drive the module.
 - (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.
 - (3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is even pixel and the second pixel is odd pixel.

5.6 LVDS INTERFACE

	SIGNAL	TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER THC63LVDF84A		TFT CONTROL INPUT
		PIN	INPUT	Host	TFT-LCD	PIN	OUTPUT	
24bit	R0	51	TxIN0	TA OUT0+	Rx 0+	27	Rx OUT0	R0
	R1	52	TxIN1			29	Rx OUT1	R1
	R2	54	TxIN2			30	Rx OUT2	R2
	R3	55	TxIN3	TA OUT0-	Rx 0-	32	Rx OUT3	R3
	R4	56	TxIN4			33	Rx OUT4	R4
	R5	3	TxIN6	TA OUT1+	Rx 1+	35	Rx OUT6	R5
	G0	4	TxIN7			37	Rx OUT7	G0
	G1	6	TxIN8			38	Rx OUT8	G1
	G2	7	TxIN9	TA OUT1-	Rx 1-	39	Rx OUT9	G2
	G3	11	TxIN12			43	Rx OUT12	G3
	G4	12	TxIN13	TA OUT2+	Rx 2+	45	Rx OUT13	G4
	G5	14	TxIN14			46	Rx OUT14	G5
	B0	15	TxIN15			47	Rx OUT15	B0
	B1	19	TxIN18	TA OUT2-	Rx 2-	51	Rx OUT18	B1
	B2	20	TxIN19			53	Rx OUT19	B2
	B3	22	TxIN20	TA OUT3+	Rx 3+	54	Rx OUT20	B3
	B4	23	TxIN21			55	Rx OUT21	B4
	B5	24	TxIN22			1	Rx OUT22	B5
	DE	30	TxIN26	TA OUT3-	Rx 3-	6	Rx OUT26	DE
	R6	50	TxIN27			7	Rx OUT27	R6
	R7	2	TxIN5	TA OUT3-	Rx 3-	34	Rx OUT5	R7
	G6	8	TxIN10			41	Rx OUT10	G6
	G7	10	TxIN11			42	Rx OUT11	G7
	B6	16	TxIN16	TA OUT3-	Rx 3-	49	Rx OUT16	B6
	B7	18	TxIN17			50	Rx OUT17	B7
RSVD 1	25	TxIN23			2	Rx OUT23	Not connect	
RSVD 2	27	TxIN24			3	Rx OUT24	Not connect	
RSVD 3	28	TxIN25			5	Rx OUT25	Not connect	
	DCLK	31	TxCLK IN	TxCLK OUT+	RxCLK IN+	26	RxCLK OUT	DCLK
				TxCLK OUT-	RxCLK IN-			

R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes: (1) RSVD (reserved) pins on the transmitter shall be "H" or "L".

5.7 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
	Cyan	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	Magenta	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red (1)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0		
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0		
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	Green (253)	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0		
	Green (254)	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0		
	Green (255)	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0		
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0		
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0		
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1		

Note: (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

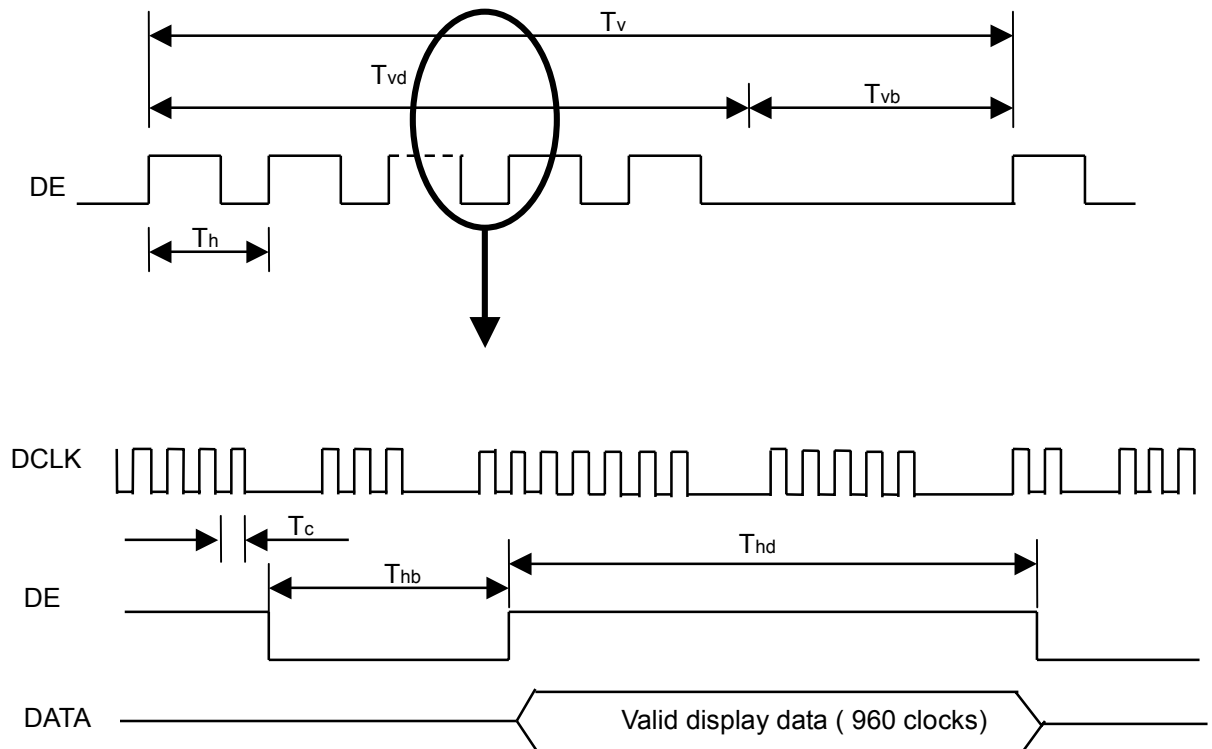
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	(60)	74	(80)	MHz	
	Input cycle to cycle jitter	Trcl	-	-	200	ps	-
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	
	Hold Time	Tlvhd	600	-	-	ps	
Vertical Active Display Term	Frame Rate	Fr5	47	50	53	Hz	(2)
		Fr6	57	60	63	Hz	(3)
	Total	Tv	(1115)	1125	(1135)	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	-
Horizontal Active Display Term	Blank	Tvb	(35)	45	(55)	Th	-
	Total	Th	(2100)	2200	(2300)	Tc	Th=Thd+Thb
	Display	Thd	1920	1920	1920	Tc	-
Horizontal Active Display Term	Blank	Thb	(180)	280	(380)	Tc	-

Note: (1) Since this module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

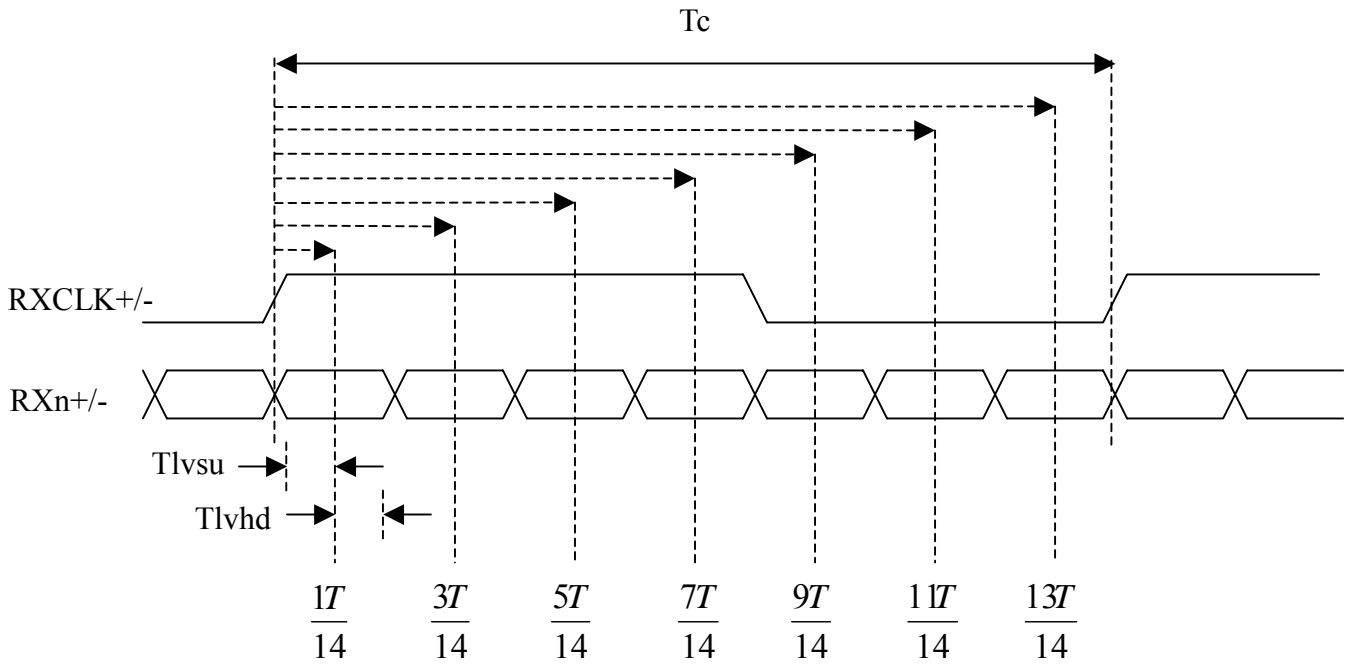
(2) ODSEL = H. Please refer to 5.1 for detail information.

(3) ODSEL = L. Please refer to 5.1 for detail information.

INPUT SIGNAL TIMING DIAGRAM

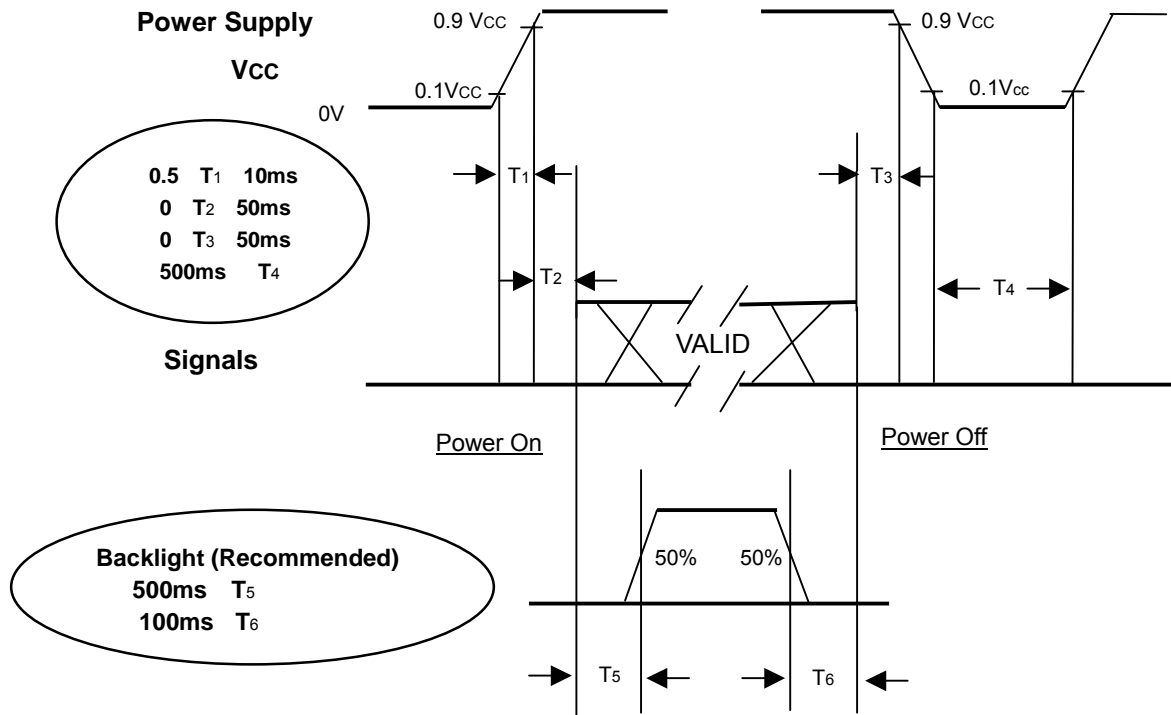


LVDS INPUT INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should follow the diagram below.



Power ON/OFF Sequence

- Note :
- (1) The supply voltage of the external system for the module input should follow the definition of V_{CC}.
 - (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.
 - (3) In case of V_{CC} is in off level, please keep the level of input signals on the low or high impedance.
 - (4) T₄ should be measured after the module has been fully discharged between power off and on period.
 - (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	5.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I _L	5.2±0.5	mA
Oscillating Frequency (Inverter)	F _L	50±1	KHz
Frame Rate	F _r	60	Hz

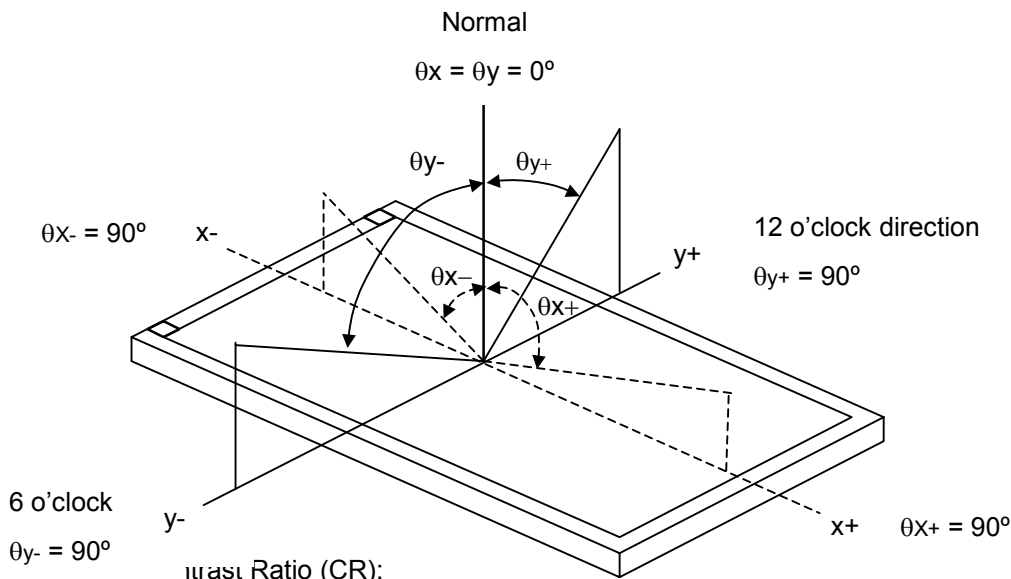
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note	
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing Normal Angle	TBD	1100	-	-	Note (2)	
Response Time		Gray to Gray average		-	6.5	TBD	ms	Note (3)	
Center Luminance of White		L _C		TBD	(500)	-	cd/m ²	Note (4)	
Average Luminance of White		L _{Ave}		TBD	(450)	-	cd/m ²	Note (4)	
White Variation		δW		-	-	1.3	-	Note (7)	
Cross Talk		CT		-	-	4.0	%	Note (5)	
Color Chromaticity	Red	Rx		TBD	TBD	TBD	-	Note (6)	0.651
		Ry							0.331
	Green	Gx							0.274
		Gy							0.595
	Blue	Bx	0.142						
		By	0.067						
	White	Wx	0.285						
		Wy	0.293						
Viewing Angle	Horizontal	θ_{x+}	CR≥20	80	88	-	Deg.	Note(1)	
		θ_{x-}							
	Vertical	θ_{y+}							
		θ_{y-}							

Note (1) Definition of Viewing Angle (θ_x, θ_y):

Viewing angles are measured by Eldim EZ-Contrast 160R



Note (2)

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{255} / L_0$$

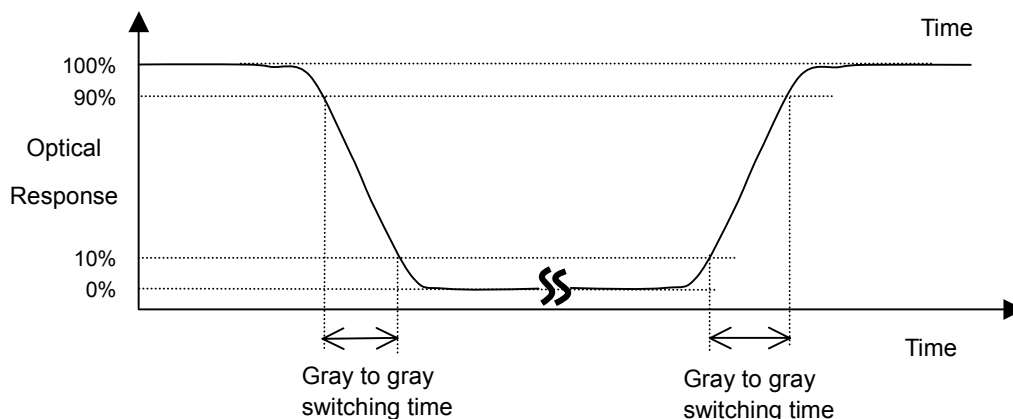
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

$$CR = CR (X)$$

CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7).

Note (3) Definition of Gray to Gray Switching Time:



The driving signal means the signal of gray level 0, 63, 127, 191, 255.

Gray to gray average time means the average switching time of gray level 0, 63, 127, 191, 255 to each other.

Note (4) Definition of Luminance of White (L_C, L_{AVE}):

Measure the luminance of gray level 255 at center point and 5 points

$$L_C = L(5)$$

$$L_{AVE} = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$$

L(x) is corresponding to the luminance of the point X at the figure in Note (7).

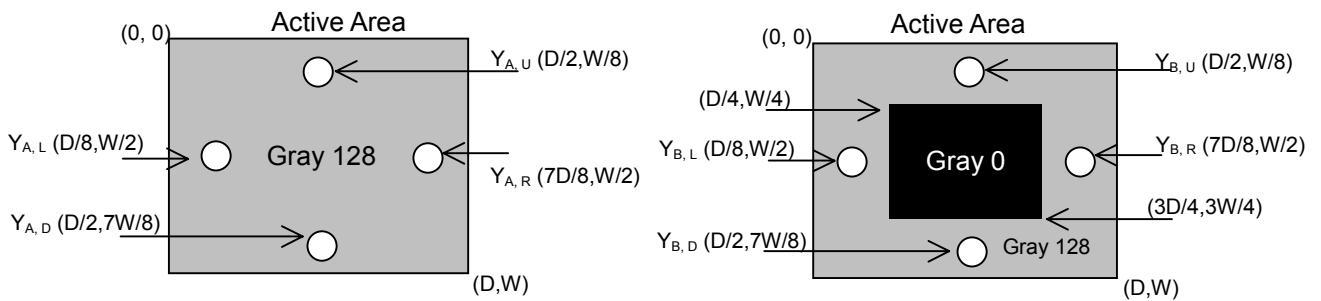
Note (5) Definition of Cross Talk (CT):

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where:

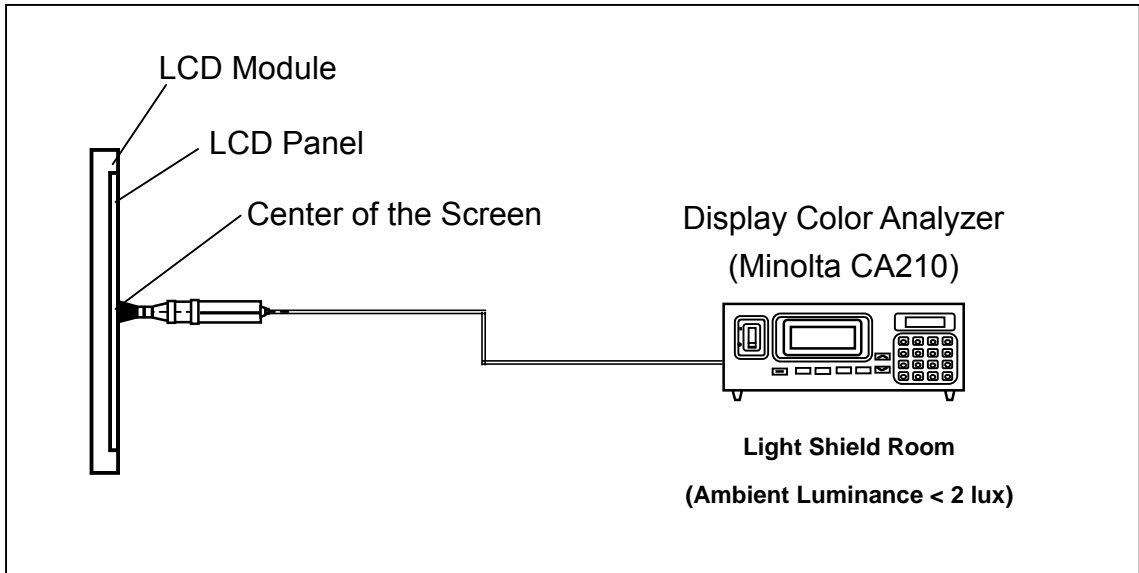
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



Note (6) Measurement Setup:

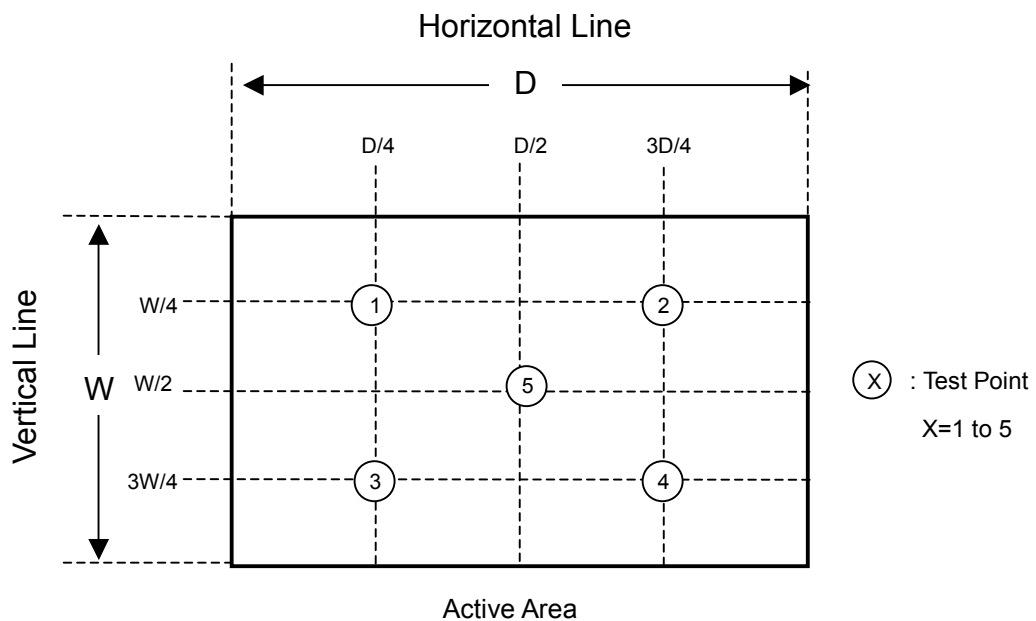
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

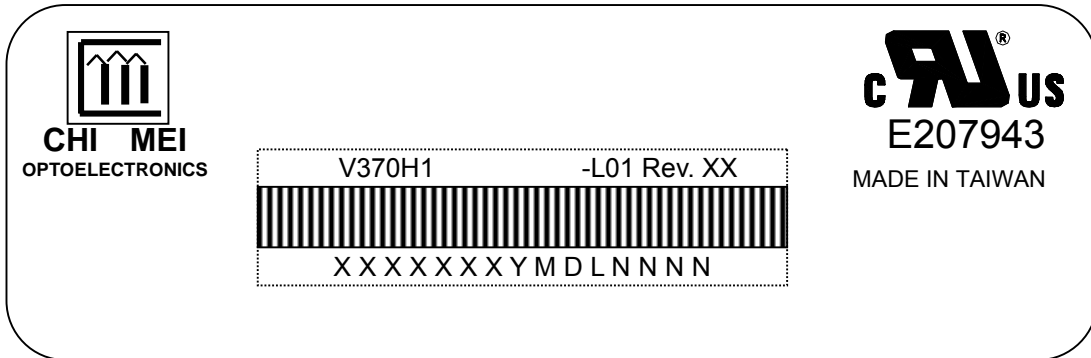
$$\delta W = \text{Maximum} [L (1), L (2), L (3), L (4), L (5)] / \text{Minimum} [L (1), L (2), L (3), L (4), L (5)]$$



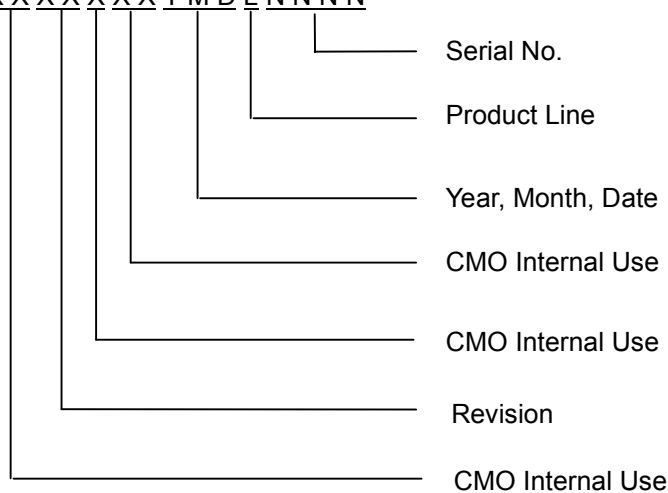
8. DEFINITION OF LABELS

8.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: V370H1-L01
- (b) Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.
- (c) Serial ID: XXXXXXXXYMDLNNNN



Serial ID includes the information as below:

- (a) Manufactured Date: Year: 0~9, for 2000~2009
 Month: 1~9, A~C, for Jan. ~ Dec.
 Day: 1~9, A~Y, for 1st to 31st, exclude I, O, and U.
- (b) Revision Code: Cover all the change
- (c) Serial No.: Manufacturing sequence of product
- (d) Product Line: 1 -> Line1, 2 -> Line 2, ...etc.

9. PACKAGING

9.1 PACKING SPECIFICATIONS

- (1) 3 LCD TV modules / 1 Box
- (2) Box dimensions : 1048(L) X 345 (W) X 676 (H)
- (3) Weight : approximately 33Kg (3 modules per box)

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

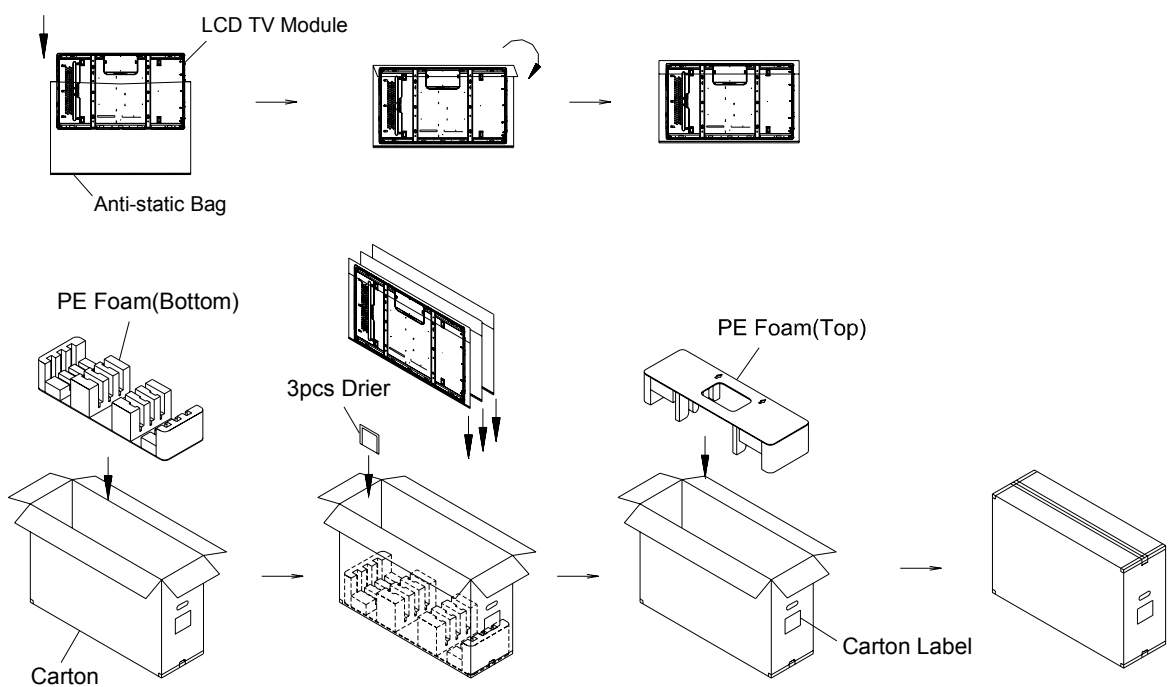


Figure.9-1 packing method

Corner Protector:L1350*50mm*50mm
L1000*50mm*50mm
Pallet:L1100*W1100*H140mm
Corrugated Fiberboard:L1100*W1100mm
Pallet Stack:L1100*W1100*H1500mm
Gross:218kg

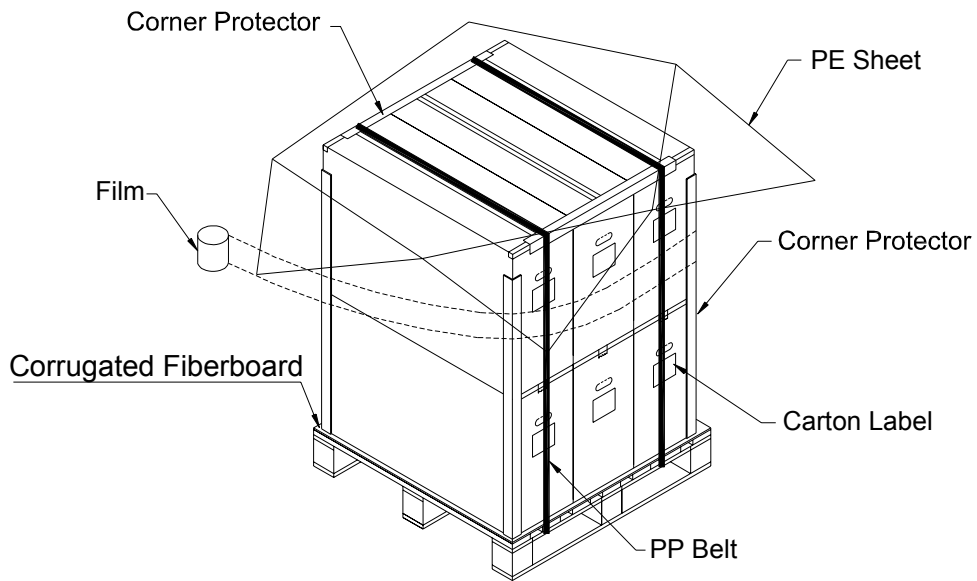


Figure. 9-2 Packing method

10. PRECAUTIONS

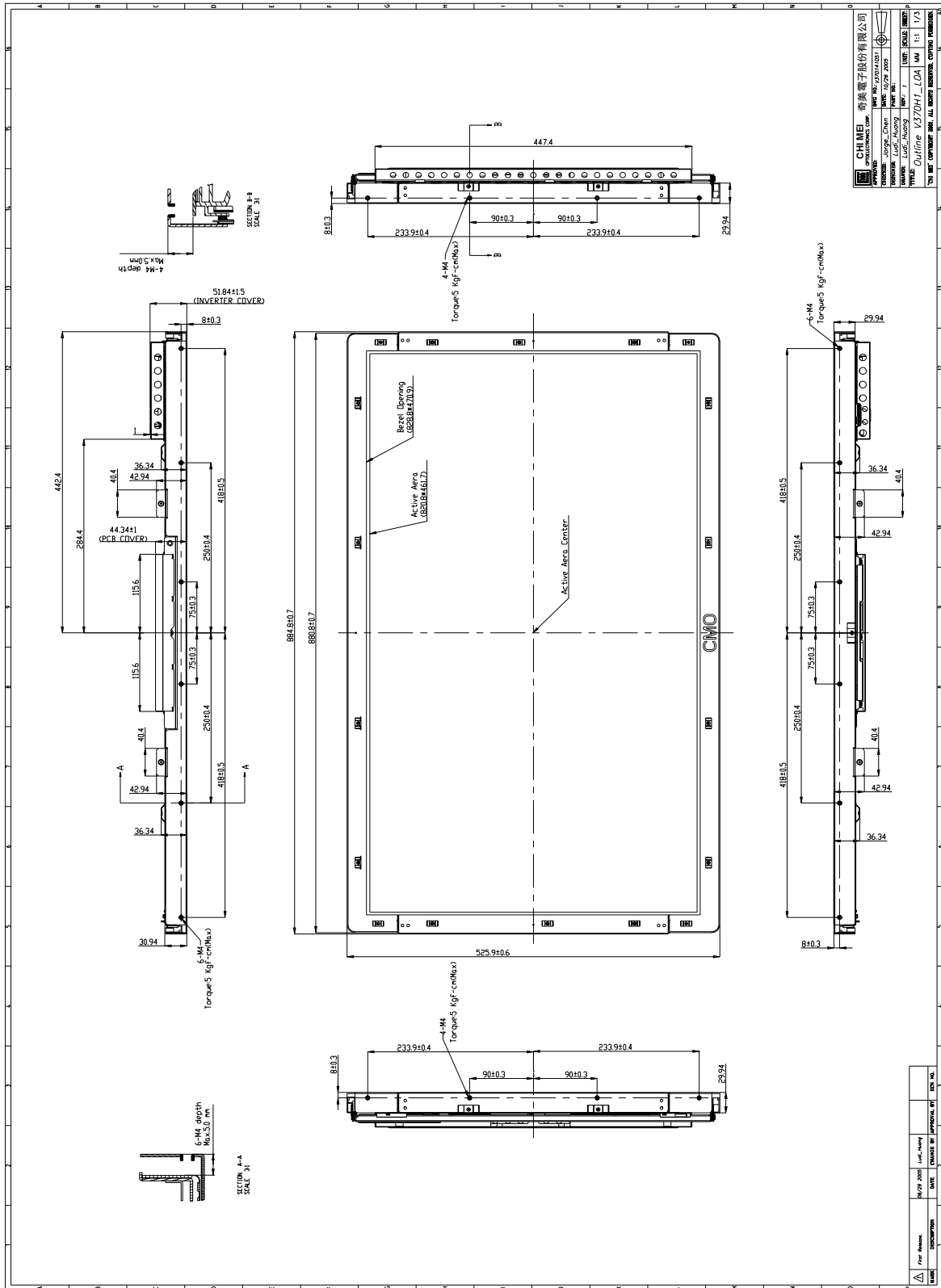
10.1 ASSEMBLY AND HANDLING PRECAUTIONS

- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.
- (4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- (5) Do not plug in or pull out the I/F connector while the module is in operation.
- (6) Do not disassemble the module.
- (7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (8) Moisture can easily penetrate into LCD module and may cause the damage during operation.
- (9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.
- (10) When ambient temperature is lower than 10°C, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

10.2 SAFETY PRECAUTIONS

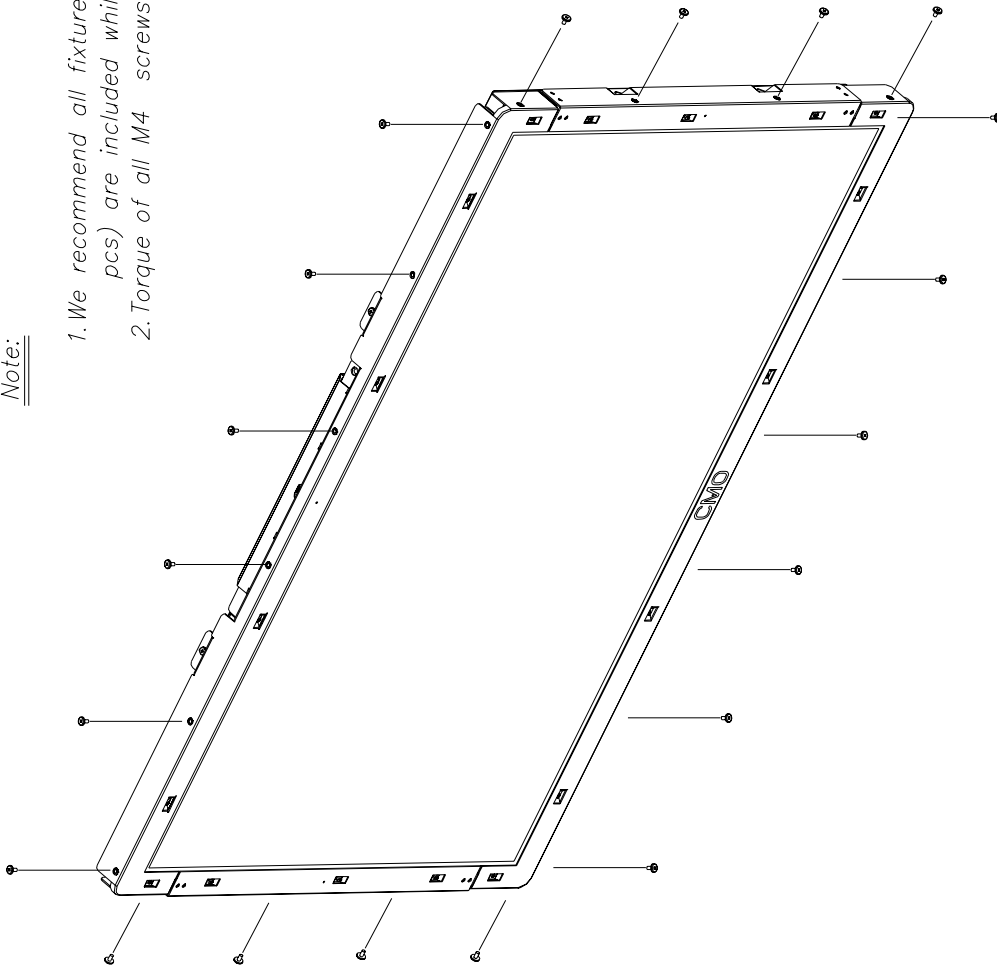
- (1) The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.

11. MECHANICAL CHARACTERISTIC



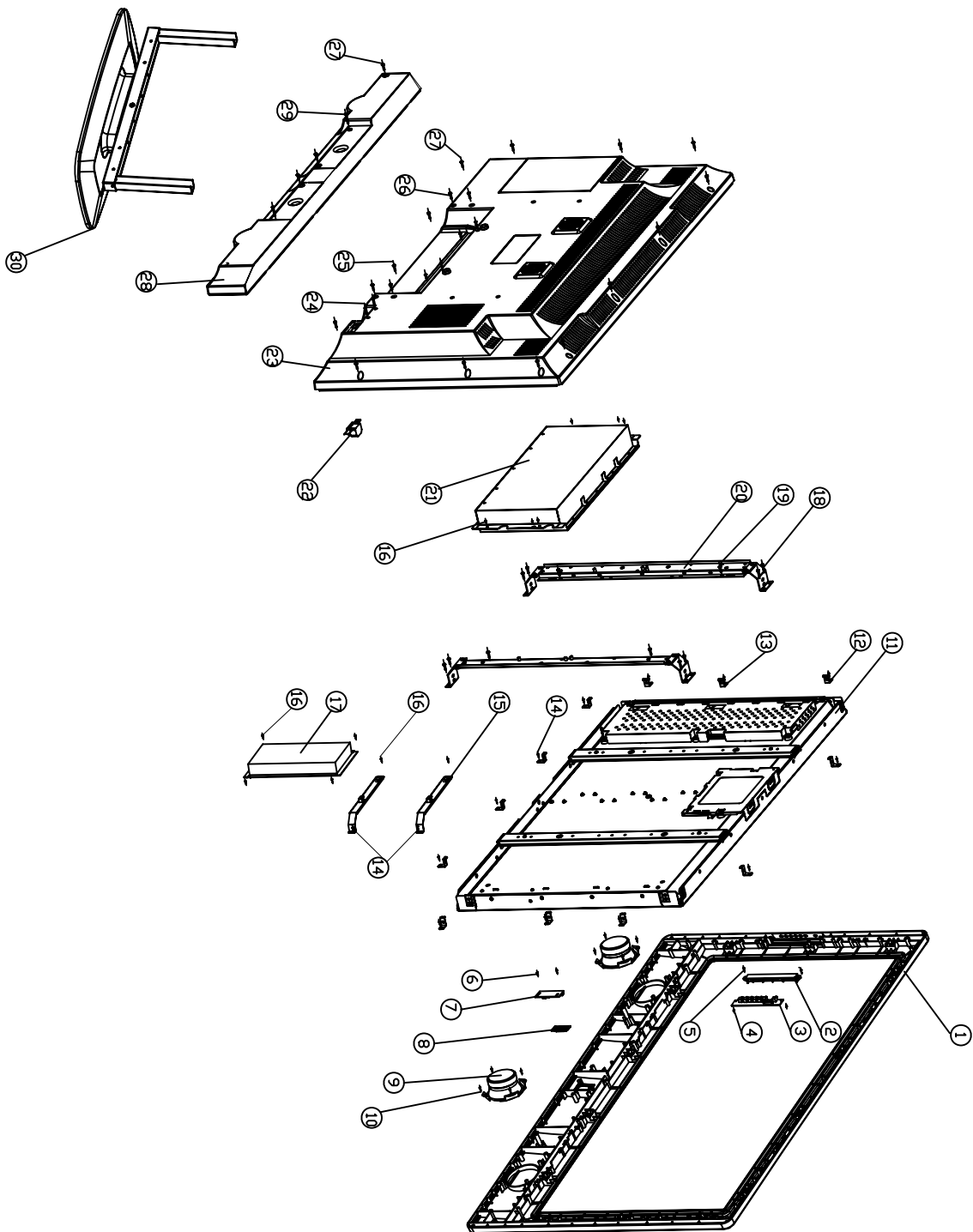
Note:

1. We recommend all fixture screws(20 pcs) are included while assembling.
2. Torque of all M4 screws are 5kgf-cm(MAX.)



CHI MEI 奇美電子股份有限公司	
DESIGNER: George Chen	DATE: 12/28/2005
DRAWN: Lufi Huang	PART NO.
CHECKED: Lufi Huang	REV: 1
TITLE: Outline Y370H1-LOA	UNIT: SCALE: 1:1
TUNING COMMENT: REV. ALL RIGHTS RESERVED. COPYRIGHT PROTECTED.	

DATE: 09/29/2005	DESIGNED BY: Lufi Huang	CHK. NO.
DESCRIPTION:	CHANGE BY: Lufi Huang	
MARK:		



ITEM	DESCRIPTION	TYPE	QTY	REMARK
30	BASE ASSY	ASSEMBLY	1	
29	TAPPING SCREW	PART	2	
28	SPEAKER CABINET BACK	PART	1	
27	TAPPING SCREW	PART	18	
26	MACH SCREW	PART	4	
25	MACH SCREW	PART	2	
24	MACH SCREW	PART	2	
23	BACK CABINET	PART	1	
22	SOCKET ASSY	ASSEMBLY	1	
21	MAIN BIDARD ASSY	ASSEMBLY	1	
20	MAIN SUPORT	PART	2	
19	MACH SCREW	PART	4	
18	TAPPING SCREW	PART	8	
17	POWER ASSY	ASSEMBLY	1	
16	MACH SCREW	PART	12	
15	POWER SUPORT	PART	2	
14	TAPPING SCREW	PART	14	
13	*2-BKT FRD PANEL	PART	1	
12	*2-BKT FRD PANEL	PART	11	
11	37' PANEL ASSY	ASSEMBLY	1	
10	TAPPING SCREW	PART	8	
9	BURDUN SPEAKER	PART	2	
8	REMOUE LENS	PART	1	
7	REMOUE PCB	PART	1	
6	TAPPING SCREW	PART	2	
5	TAPPING SCREW	PART	2	
4	TAPPING SCREW	PART	2	
3	FUNCTION KEY PCB ASSY	ASSEMBLY	1	
2	FUNCTION KEY	PART	1	
1	FRONT CABINET	PART	1	

DRAWN.		TOLERANCE UNLESS OTHERWISE SPECIFIED	KAWA ELECTRONIC R & D CENTRE	TITLE	LCT37AE-EXP
CHECKED		0. ± 0.30	MATL.	MODEL NO.	LCT37AE
APPRD.		0.0 ± 0.10		PART NO.	A3 LCT37AE/AMAICS-B01
3rd ANGLE PROJECTION		0.00 ± 0.05	FINISH	DWG. NO.	LCT37AE/AMAICS-B01
		ANGULAR ± 0.3°		SCALE 1:10	QTY. 1
		UNIT : mm			SHEET 1 OF 1

DWG. REV./ZONE	DESCRIPTION	DATE	REVISOR

Spare part list for LCT37Z6TA

Item	Part Number	Part Description	Usage / unit	Unit	Key/Spare
1>	LCT37AEIA1CS-B01	AKAI LCT37AE(LCT37Z6TA) S-MT8206 CMO (V370H1-L0A V2.2) HORIZONTAL AC120V/60HZ USA SILVER/BLACK			
	510-L37AE02-01AK	FLAT CARTON BOX AKAI LCT37Z6TA S-MT8206 USA K	1.000000	Piece	K
2>	580-L37AE1A-02AP	IB E FOR AKAI LCT37Z6TA TV+ATSC NO PIP CMO MTK8206 USA	1.000000	Piece	K
3>	E3407-081001	CORD FFC P0.5 50P L=110 B-0.5-50X110-4(8)X4(8)-0.3X0.035	1.000000	Piece	K
4>	E7501-056108	REMOTE CONTROL K001 "AKAI" 44KEYS MT8206 LCT37" (W/O DVD) USA BLACK	1.000000	SET	K
5>	E7801-P02003	PCB ASSY PSU BOARD MEGMEET MLT386X FOR 37LCD AC110-240V OUTPUT 12V/8V/24V 250W	1.000000	SET	K
6>	771EL37AE02-01	MAIN PCB ASS'Y S-MT8206 FOR LCT37AE CMO USA	1.000000	SET	K
7>	771S42D102-02	ATSC TUNER PCB ASS'Y (MT5111CE) W/O MAX3232	1.000000	SET	K
8>	200-L37AE02-01AA	CABINET FRONT MATT BLACK/SILVER LCT37AE CMO A	1.000000	Piece	S
9>	202-L37AD15-01AA	CABINET BACK LCT37AD	1.000000	Piece	S
10>	206-L37AE01-01AR	SPEAKER BACK COVER BLACK LCT37AE R	1.000000	Piece	S
11>	231-L32AD01-04R	BASE COVER BLACK(P320-605870-01)	1.000000	Piece	S
12>	269-42SD01-01L	REMOTE RECEIVE LENS	1.000000	Piece	S
13>	300-L37AE03-02C	POLYFOAM BOTTOM FOR RS	1.000000	Piece	S
14>	300-L37AE04-02C	POLYFDAM TOP FOR RS	1.000000	Piece	S
15>	310-030404-01	POLYBAG 110MMX80MMX0.04MM	2.000000	Piece	S
16>	310-041204-01V	POLYBAG 4"X12"X0.04 AV	1.000000	Piece	S
17>	310-102004-01T	POLYBAG FOR 32" 37" METAL CROS SBEAM	1.000000	Piece	S
18>	310-111404-07V	POLYBAG 11"X14"X0.04 FV	1.000000	Piece	S

Spare part list for LCT37Z6TA

19>	310-142804-01T	POLYBAG FOR 32" 37" STAND T 14"X28"X0.04	1.000000	Piece	S
20>	310-444750-07V	POLYBAG 44X47X50	1.000000	Piece	S
21>	370-42D102-01	PAD CORD SPONG FOR SPK	1.000000	Piece	S
22>	370-L32AD01-01Y	RUBBER FOOT 20X6 L32AD Y	6.000000	Piece	S
23>	388-42SB04-01H	POWER PLATE SANSUI 42SB H	1.000000	Piece	S
24>	420-L32AD11-01	BOTTOM PLATE	1.000000	Piece	S
25>	426-L37AD02-01S	AC JACK BRACKET	1.000000	Piece	S
26>	429-L32AB13-01	L SHEET	2.000000	Piece	S
27>	429-L32AB56-01	"U" TOP CROSSBEAM LCT32AD	1.000000	Piece	S
28>	429-L32AD0E-01	SECURE LEG	2.000000	Piece	S
29>	429-L37AD0B-01S	POWER SUPPORT	2.000000	Piece	S
30>	436-L32AB0G-01S	TERMINAL SHEET FOR COMPONENT X2	1.000000	Piece	S
31>	481-L32AB06-01S	SHIELDING BOTTOM MT8202	1.000000	Piece	S
32>	483-L32AB32-01S	SHIELDING COVER	1.000000	Piece	S
33>	522-421D01-01	MASKING PAPER	1.000000	Piece	S
34>	553-002007-25A	SHIELD GASKET 20X7X2.5MM W/ CONDUCTIVE ADHESIVE	1.000000	Piece	S
35>	560-L37AE01-02AP	MODEL LABEL AKAI LCT37Z6TA S- MT8206 USA P	1.000000	Piece	S
36>	563-119-	SERIAL NO. LABEL	1.000000	Piece	S
37>	568-P46T02-02	WARNING LB ENG 42SF NIL	1.000000	Piece	S
38>	578-L37AD01-01AP	FUNCTION SHEET FOR TERMINAL LCT37" S-MT8202 USA P	1.000000	Piece	S

Spare part list for LCT37Z6TA

39>	579-42D102-09	SERIAL NO/BAR CODE LABEL 42D1	1.000000	Piece	S
40>	579-42D105-01	PROTECTIVE EARTH LABEL FOR ESA 42TD1	1.000000	Piece	S
41>	579-L27AD09-01	CAUTION LABEL ENG AKAI	1.000000	Piece	S
42>	579-L32AD09-02AP	FCC STATEMENT LABEL 77X20MM	1.000000	Piece	S
43>	579-L37AD05-02AP	SCREW LABEL FOR LCT37AD WALL BRACKET	1.000000	Piece	S
44>	579-L37AD05-03AP	SCREW LABEL FOR LCT37AD SQUARE BASE COVER	1.000000	Piece	S
45>	579-L37AE01-01AP	BAR CODE LABEL AKAI LCT37Z6TA USA	2.000000	Piece	S
46>	590-L37AE01-01AP	WARRANTY CARD AKAI LCT37Z6TA USA	1.000000	Piece	S
47>	593-L37AE01-01AP	INSERTION CARD AKAI LCT37Z6TA USA	1.000000	Piece	S
48>	599-L37AE01-01AP	IB SHEET E FOR LCT37AE STAND USA (RS)	1.000000	Piece	S
49>	599-L42AE02-01AP	IB SHEET E FOR LCT37AE/LCT42AE INITIAL SETUP USA	1.000000	Piece	S
50>	E3219-002003	EI I LET EMI FILTER WIT WIRES IOSSI-R- Q(B) HIGH&LOW	1.000000	Piece	S
51>	E3404-157004	AC CORD UL 1.88M (YY-3/ST3 YUNBIAO)	1.000000	Piece	S
52>	E3421-925118	WIRE ASSY 8P2.5/7P2.0 L170MM 5V 12V SIGNAL POWER MT8202	1.000000	Piece	S
53>	E3421-925127	WIRE ASSY TJC3-2Y L860 SPK-R MT8202	1.000000	Piece	S
54>	E3421-925139	WIRE ASSY TJC3-3Y L760MM LCD37" MT8202 SPK-L	1.000000	Piece	S
55>	E3421-925151	WIRE ASSY 16P/2.0/11P/2.5/10P/2.5/8P/2.0 FOR MT8202 5V/12V/9V	1.000000	Piece	S
56>	E3421-925153	WIRE ASSY 250MM 3WIRES 20# 1617 FOR POWER IN PUT	1.000000	Piece	S
57>	E3421-926112	WIRE ASSY L=540 2.0/2.5 4P FOR 32LCD W/EMI	1.000000	Piece	S
58>	E3461-000115	WIRE ASSY 10P2.5/12P2.0 L500MM INVERTER MT8202 LCT47" CMO	1.000000	Piece	S

Spare part list for LCT37Z6TA

59>	E3461-064042	WIRE ASSY 1H2.5-2H2.0 20099 L350 7P/5P FOR MT8202 37" STANDBY	1.000000	Piece	S
60>	E3471-000072	WIRE WS SHIELD FOR MT8202 MICO KEY 13P/8P+5P L650/L750MM W/O EMI	1.000000	Piece	S
61>	E3471-000075	WIRE WS SHIELD F1-R51S-H L300MM LCT37&47 CMO MT8202 LVDS NEW	1.000000	Piece	S
62>	E4801-124001	SPEAKER 8 OHM 10W D3" YD78-1	2.000000	Piece	S
63>	E6203-37CD01	DISPLAY LCD 37" CMO WXGA V370H1- LOA C2	1.000000	Piece	S
64>	E7301-010002	BATTERY AAA R03P1.5V <2>	2.000000	Piece	S
65>	771BL42AE02-01	IR RECEIVE PCB ASS'Y FOR LCT42AE S- MT8206	1.000000	SET	S
66>	771KL42AE02-01	KEY PCB ASS'Y FOR LCT42AE S-MT8206	1.000000	SET	S

Software Upgrade

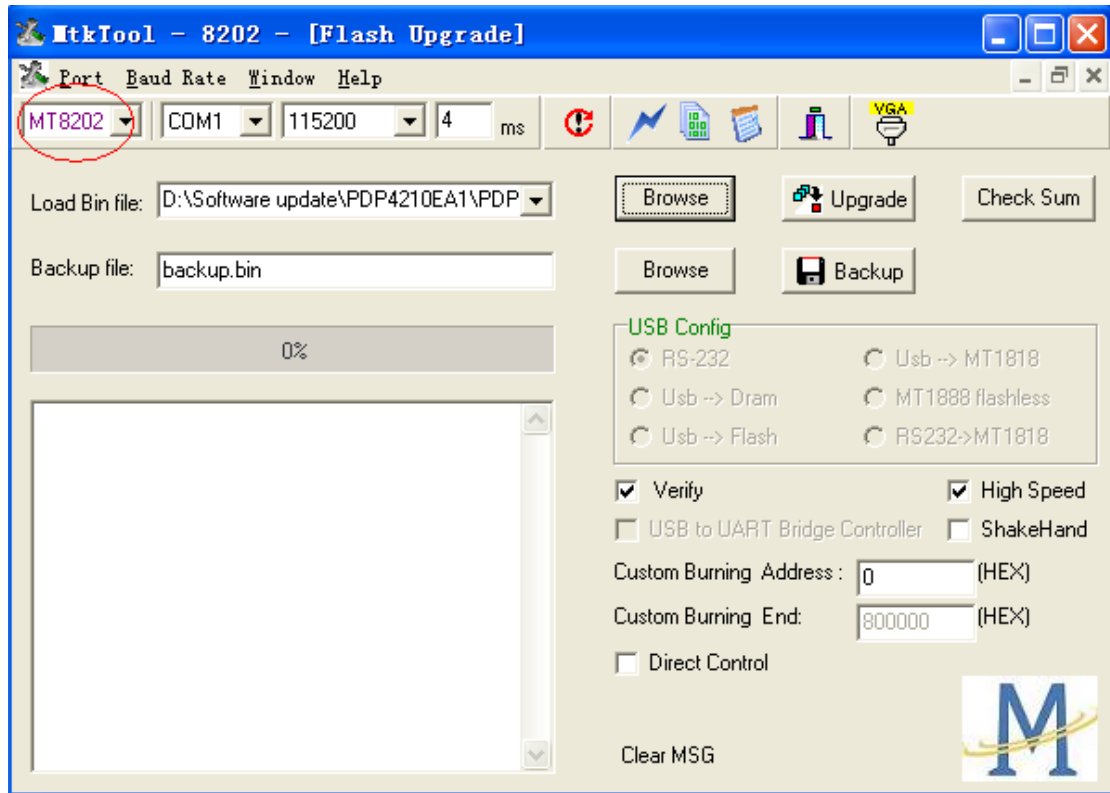
Process of update MT8206

Preparing :

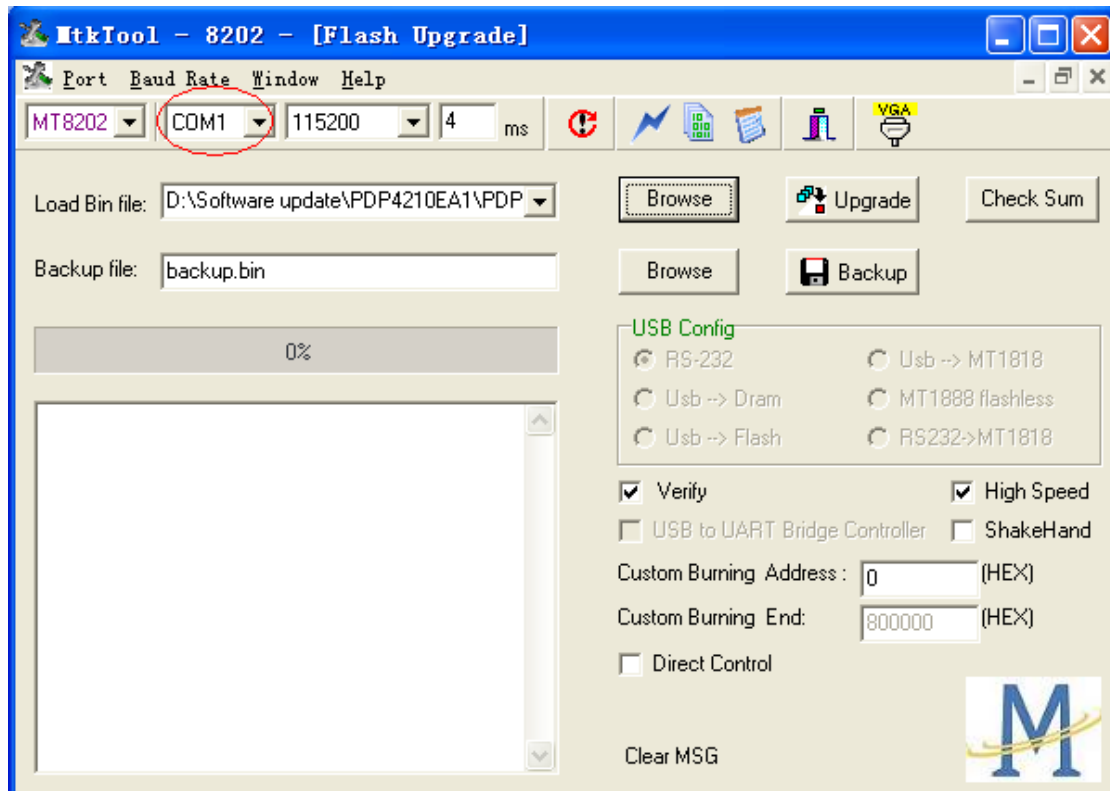
1. Connect the Plasma/LCD TV and PC with the **Software Upgrade Board**. Please find the details for connecting **referring to the appendix at the end of this file**.
2. Store the MtkTool into the PC .

Downloading :

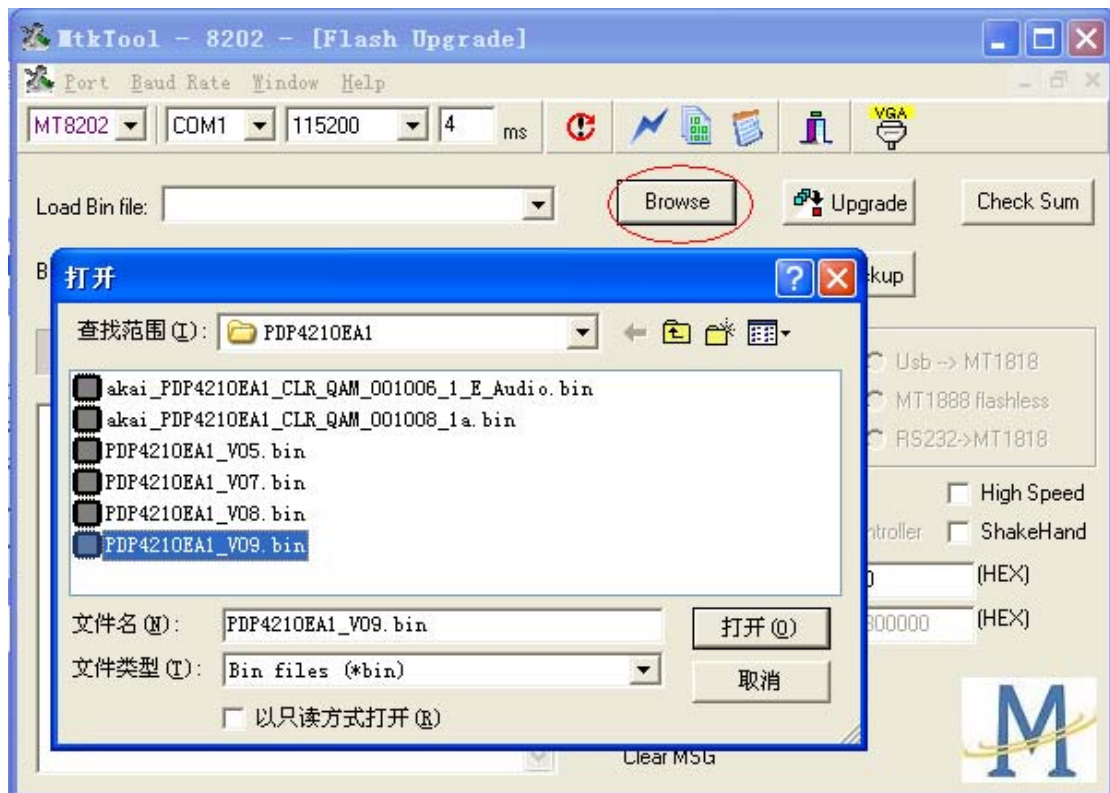
3. Turn on AC power of the TV and then press the button “standby” of the remote control . The image could be found on the screen of the Plasma TV while the color of the power indicator is green . (the mode of the TV will be standby mode if after turn on the main power only .)
4. Execute MTKtool and select the chipset as MT8202. (the software of MTKtool will be sent to your side)



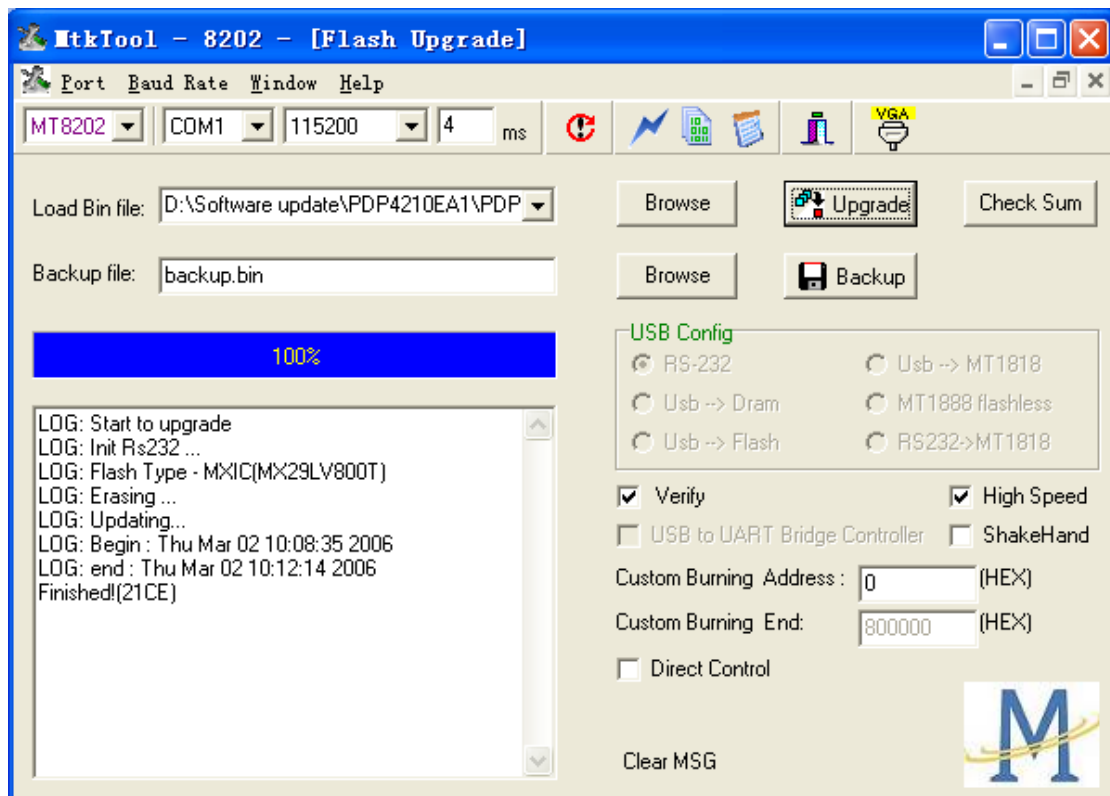
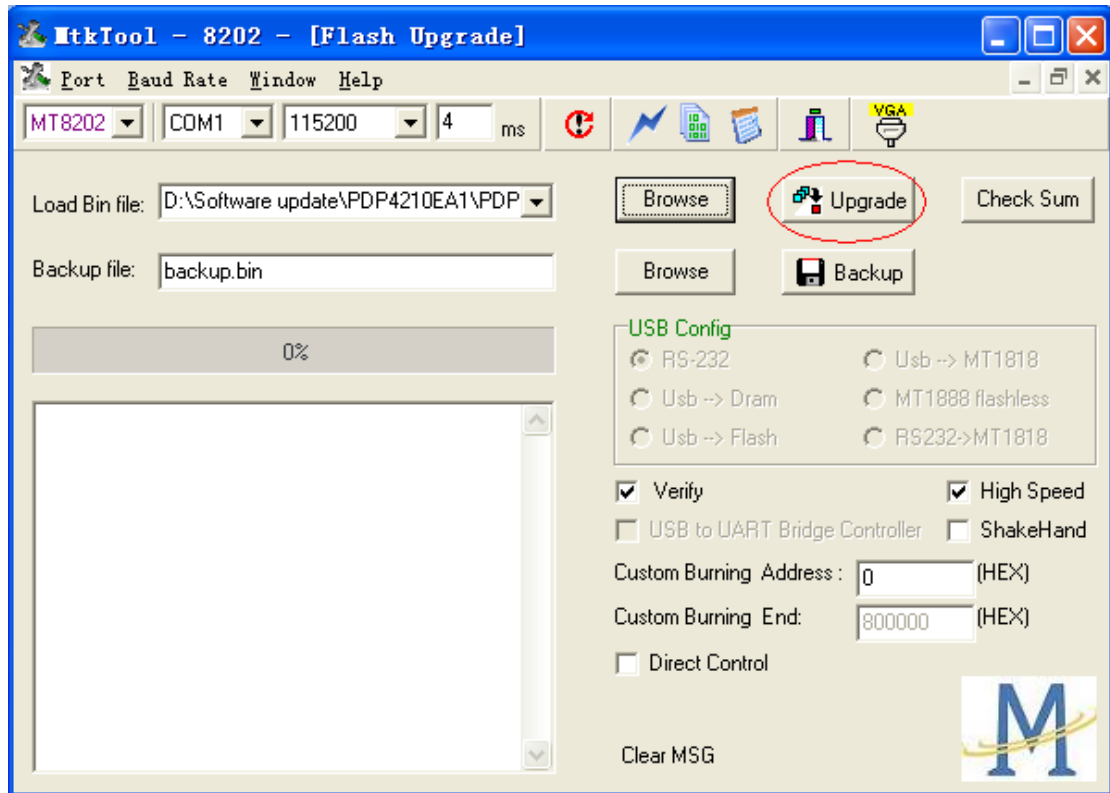
5. Select current COM port. (please try to check the COM port of your PC).



6. Choose the bit rate as 115200.
7. Select the update binary by pressing browse button. For example, the binary file name is PDP4210EA1_V09.bin. (this update firmware will be sent to your side)



8. Press Upgrade button and start update process.



9. The update process is successful as the progress bar is 100%. After the update process is ok,

turn off power and wait indicator light is off. Turn on power and TV can work.

Checking

It is needed to check the version of the firmware for MT8202 which has been download into the Plasma TV .

Press Menu button of the remote control, following input “8202” of the remote control and OSD menu for Factory Setting is appeared on the screen .

Use the remote control and select the mode of Firmware Version and then enter the mode of Firmware Version . It is easy to be found the version of the current firmware for MT8202 is as the following : “Factory ID : PDP4210EA1_VXX ”

Appendix:

Quick Installation Guide For Software Upgrade Board

1. Parts List

- Software upgrade board x 1 (#1)
- RS232 null cable x 1 for PC (#2)
- RS232 – VGA cable (#4)
- USB cable x 1 (#5)

2. Installation for ATV upgrade

2.1 Connect RS232 cable (#2) to PC serial port



Connect another side of RS232 cable (#2) to the board (#1)



2.2 Connect RS232-VGA cable (#4) (RS232 side) to the board (#1)



Connect RS232-VGA cable (#4) (VGA side) to the TV



2.3 Connect USB cable (#5) to the board (#1)

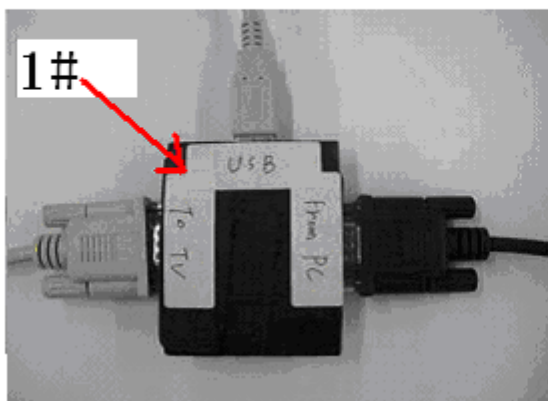


Connect another side of USB cable (#5) to PC

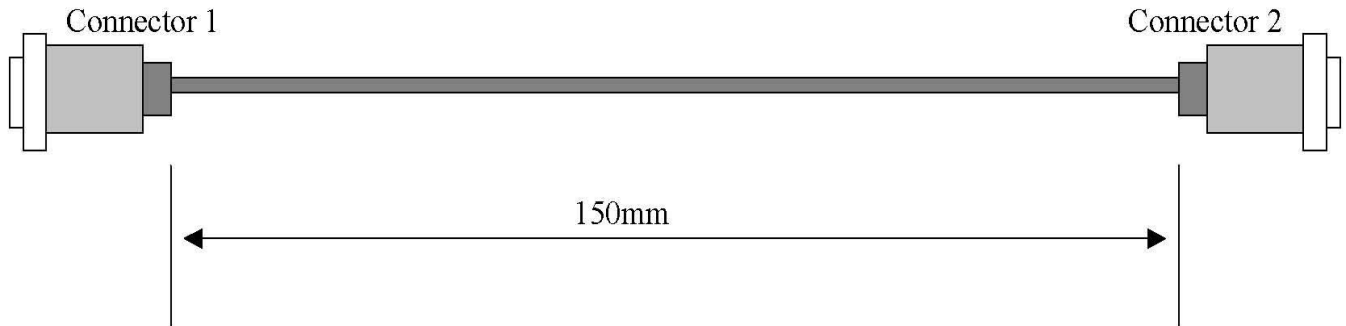


3. Cables Standard for Upgrade Board

Software upgrade board x 1 (#1)



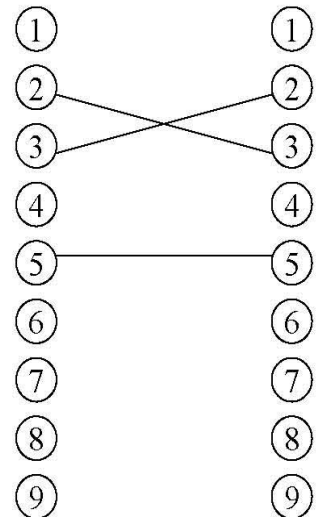
RS232 Null Cable for PC (#2)



Pin Assignment
Of DB9 Female

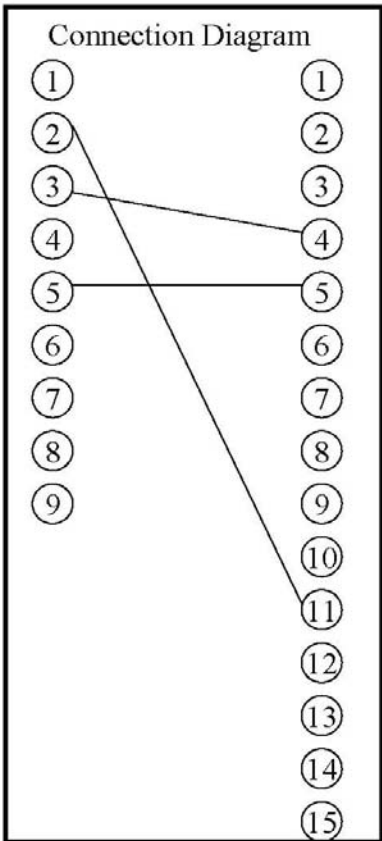
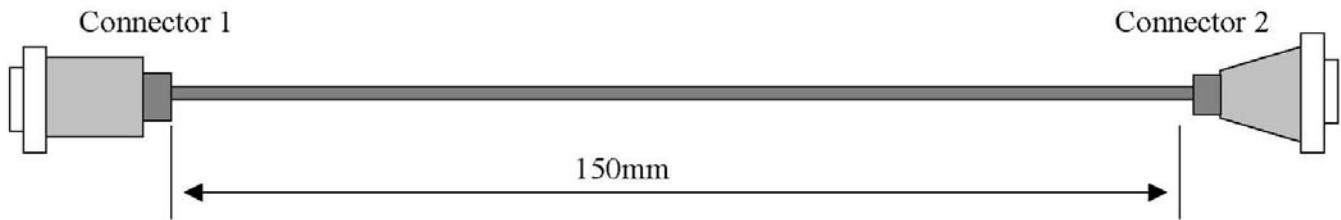


Connection Diagram



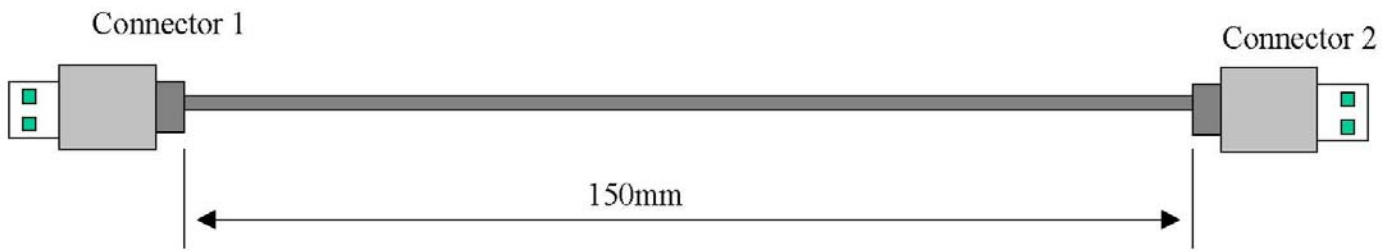
Connector 1: DB9 Female
Connector 2: DB9 Female

RS232 - VGA Cable (#4)



Connector 1: DB9 Female
Connector 2: VGA Male

USB Cable (#5)



Connector 1: Standard USB Male

Connector 2: Standard USB Male

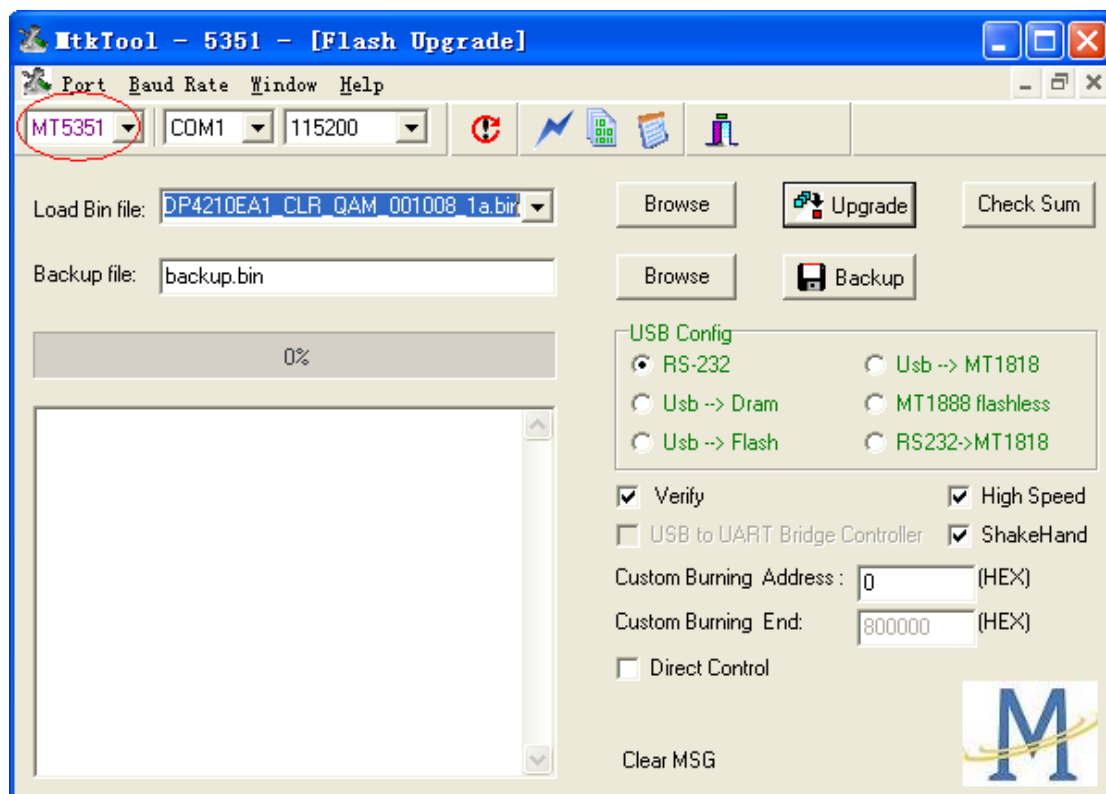
Process of update MT5351AG

Preparing :

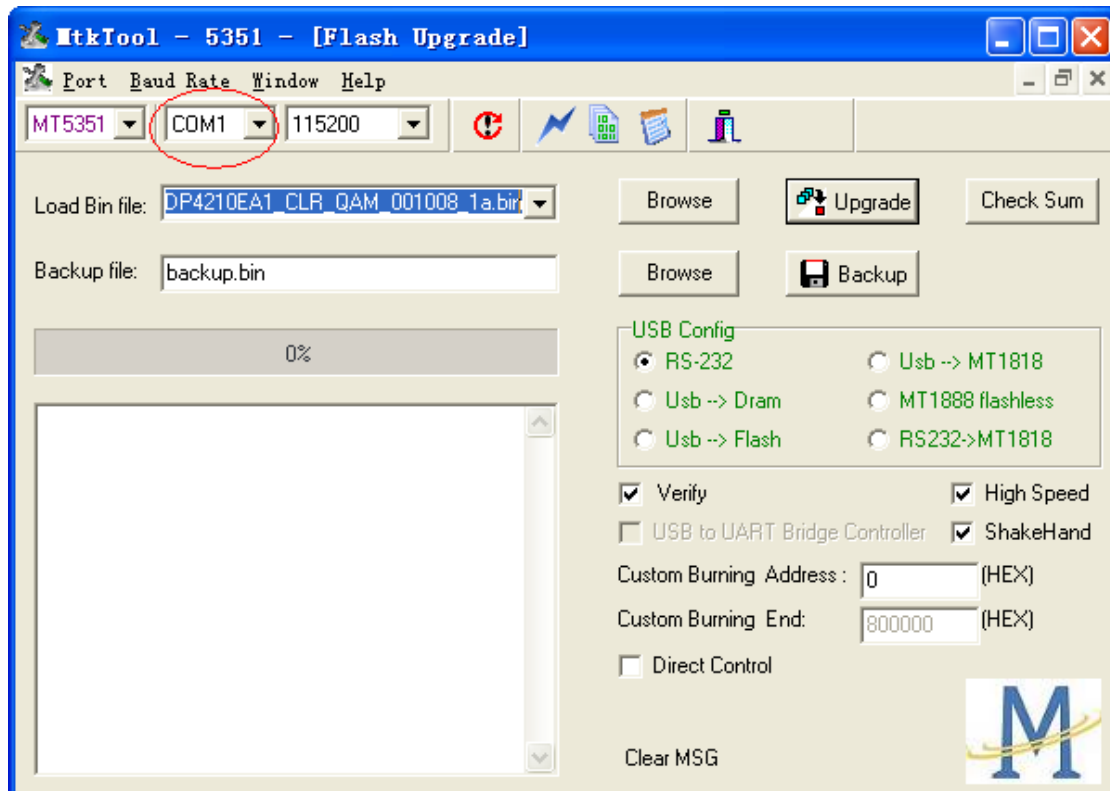
1. Connect the Plasma/LCD TV and PC with the **Software Upgrade Board**. Please find the details for connecting **referring to the appendix at the end of this file**.
2. Store the MtkTool into the PC

Downloading :

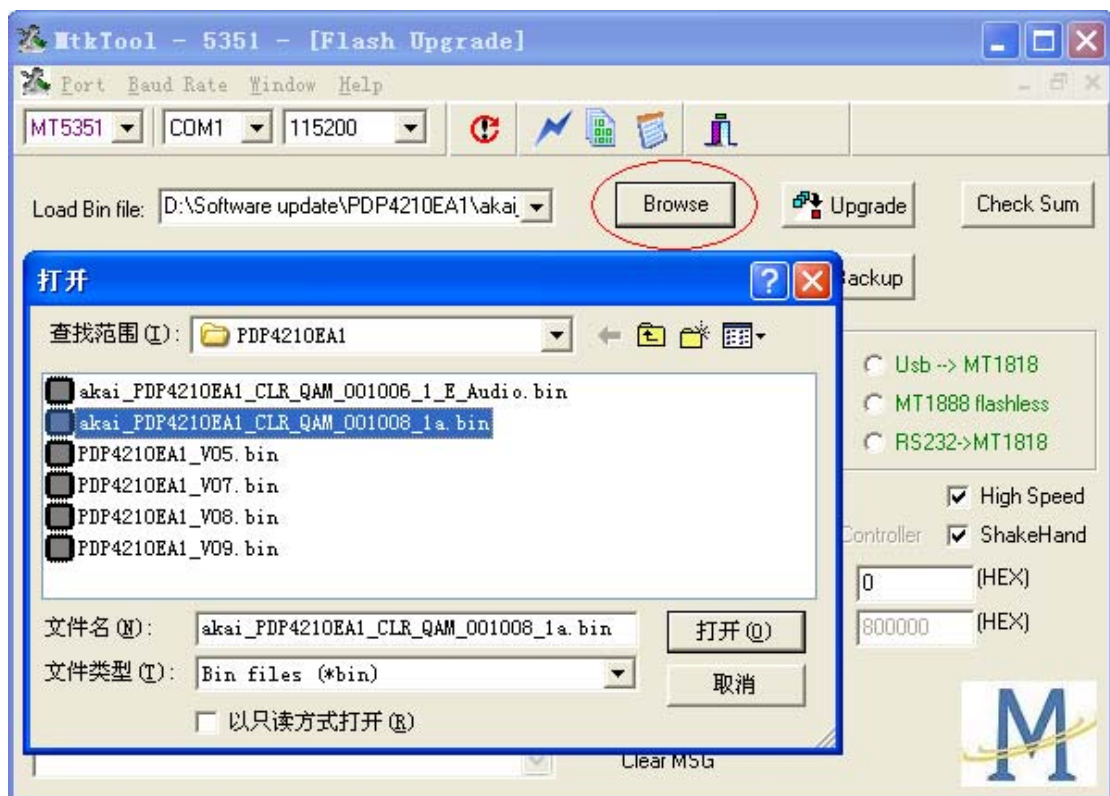
3. Turn on AC power of the TV and then press the button “standby” of the remote control . The image could be found on the screen of the Plasma TV while the color of the power indicator is green . (the mode of the TV will be standby mode if after turn on the main power only .)
4. Execute MTKtool and select the chipset as MT5351. (the software of MTKtool will be sent to your side)



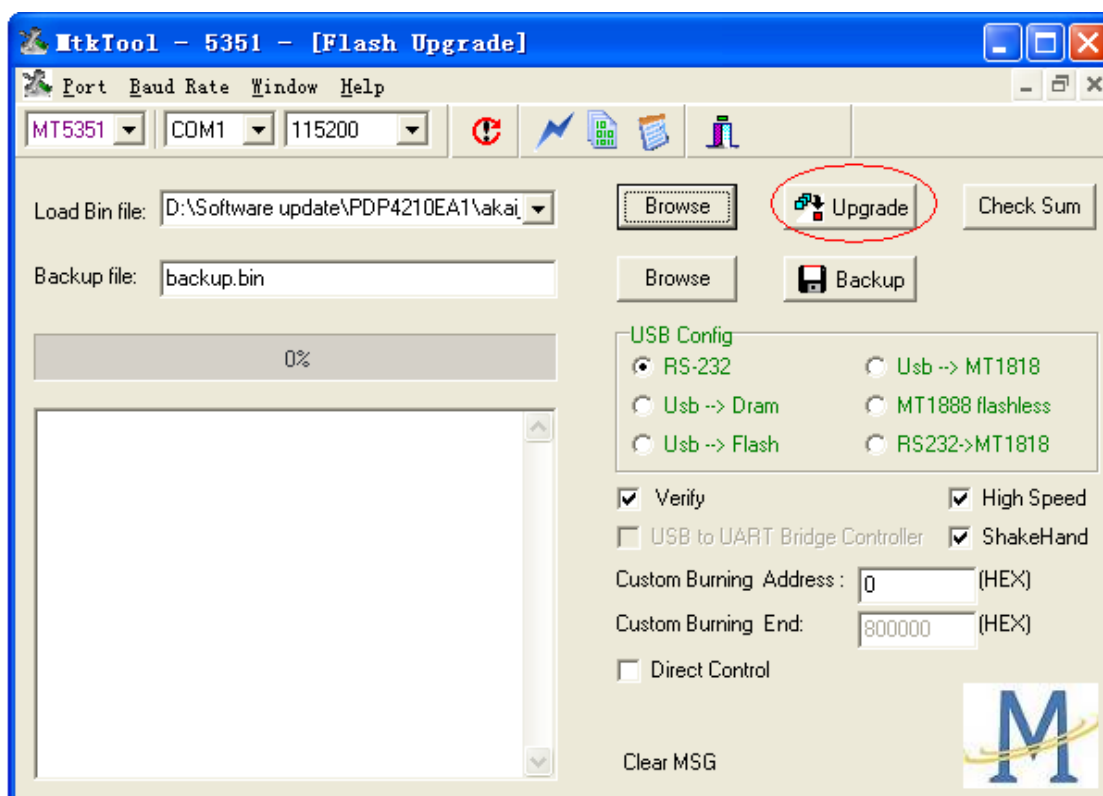
5. Select current COM port. (please try to check the COM port of your PC).



6. Choose the bit rate as 115200.
7. Select the update binary by pressing browse button. For example, the binary file name is XXXX_PDP4210EA1_000000XX_X_P.bin. (this update firmware will be sent to your side)



8. Press Upgrade button and start update process.



9. The update process is successful as the progress bar is 100%. After the update process is ok, turn off power and wait indicator light is off. Turn on power and TV can work.

Checking :

It is needed to check the version of the firmware for MT5351AG which has been download into the Plasma TV .

Press Menu button of the remote control and the main OSD menu is appeared on the screen .

Use the remote control and select the DTV menu . following input “0000” (zero , zero , zero , zero) of the remote control .Then enter the mode of factory after input the digits .

It is easy to be found the version of the current firmware for MT5351AG is “PDP4210EA1 CLA_QAM_XXXXXX_XX”under the mode of factory .

Appendix:

Quick Installation Guide For Software Upgrade Board

1. Parts List

- Software upgrade board x 1 (#1)
- RS232 null cable x 1 for PC (#2)
- RS232 null cable x 1 for DTV (#3)
- USB cable x 1 (#5)

2. Installation for DTV upgrade

2.1 Connect RS232 cable (#2) to PC serial port



Connect another side of RS232 cable (#2) to the board (#1)



2.2 Connect RS232 cable for DTV (#3) to the board (#1)



Connect another side of RS232 cable for DTV (#3) to the TV



2.3 Connect USB cable (#5) to the board (#1)

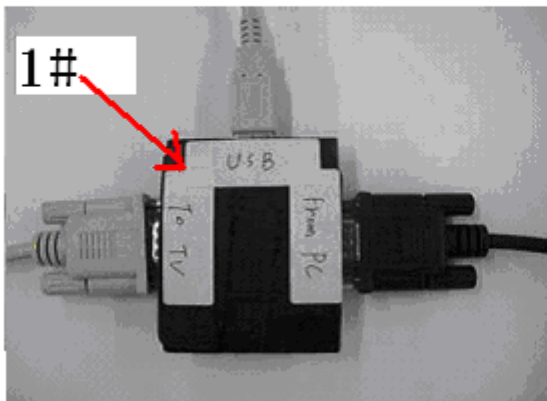


Connect another side of USB cable (#5) to PC

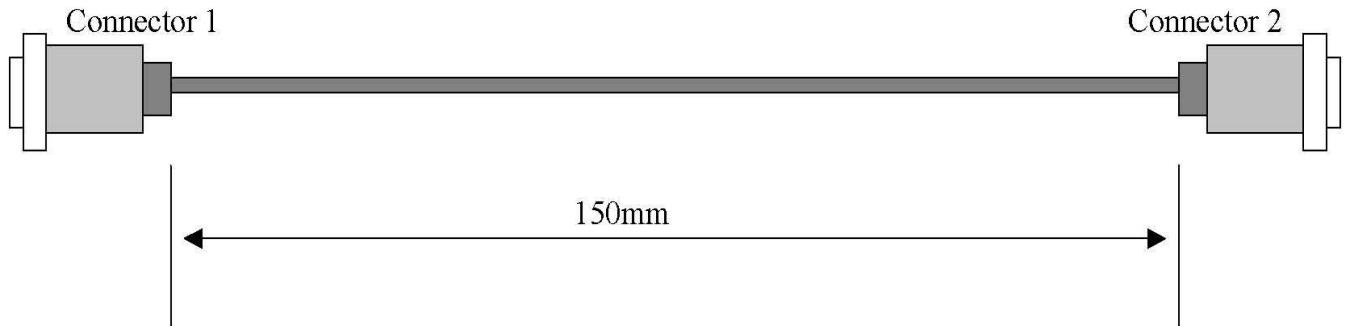


3. Cables Standard for Upgrade Board

Software upgrade board x 1 (#1)



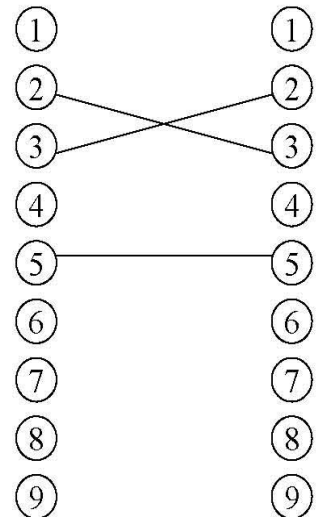
RS232 Null Cable for PC (#2)



Pin Assignment
Of DB9 Female

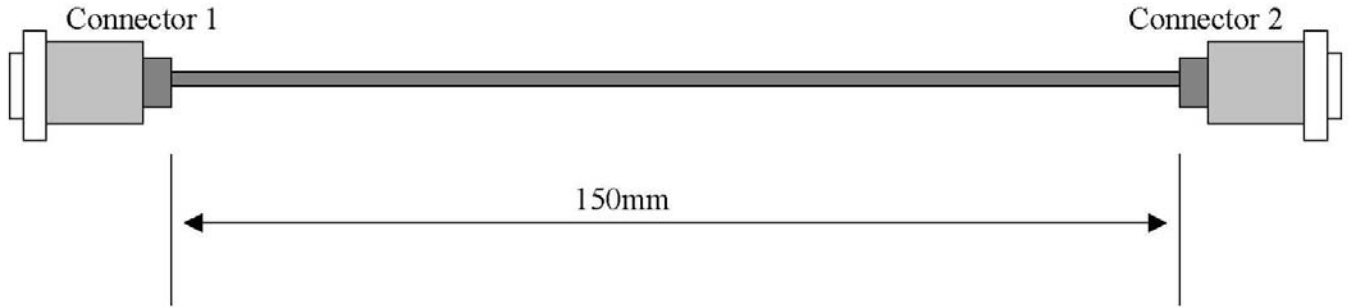


Connection Diagram

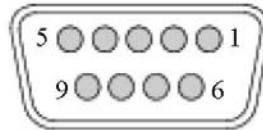


Connector 1: DB9 Female
Connector 2: DB9 Female

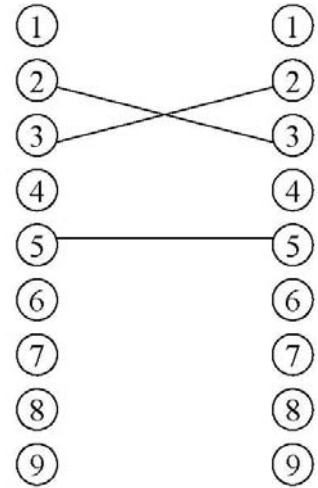
RS232 Null Cable for DTV (#3)



Pin Assignment
Of DB9 Female

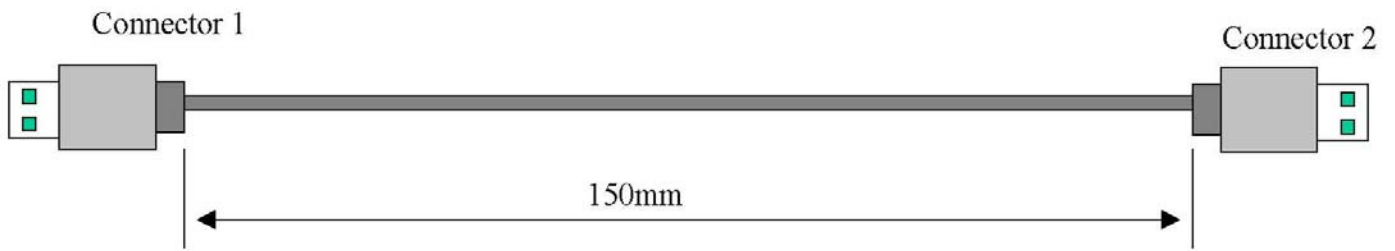


Connection Diagram



Connector 1: DB9 Female
Connector 2: DB9 Female

USB Cable (#5)



Connector 1: Standard USB Male

Connector 2: Standard USB Male